THC63LVD1023B

30Bit Color/160MHz LVCMOS to Dual Link LVDS converter

General Description

The THC63LVD1023B transmitter is designed to support FPD Link transmission between Host and Flat Panel Display up to 1080p60Hz and Dual Link transmission between Host and Flat Panel Display up to 1080p(120Hz).

The THC63LVD1023B converts 70-bit LVCMOS signals to 10-channel LVDS signals using a 7:1 serializer. The transmitter can be programmed for rising edge or falling edge clocks through a dedicated pin, and support double edge inputs.

In Dual Link, the transmit clock frequency of 160MHz, 67bits of RGB data are transmitted at an effective rate of 1.12Gbps per LVDS channel.

In Asynchronous mode, the THC63LVD1023B has 2 independent 35Bits Transmitter.

Features

- Wide dot clock range
  - LVCMOS Input: 10-160MHz
  - LVDS Output: 20-160MHz
- Flexible Input / Output mode
  - Pixel Alignment, Dual/Single Port Conversion
  - Distribution
  - Port switching in two asynchronous inputs
- Input data sampling clock edge selectable
- VESA/JEIDA LVDS data mapping support
- Pseudo Random pattern generation circuit
- Supports Reduced swing LVDS for Low EMI
- Power down mode
- 3.3V single power supply
- 144pin LQFP
- EU RoHS Compliant

Block Diagram

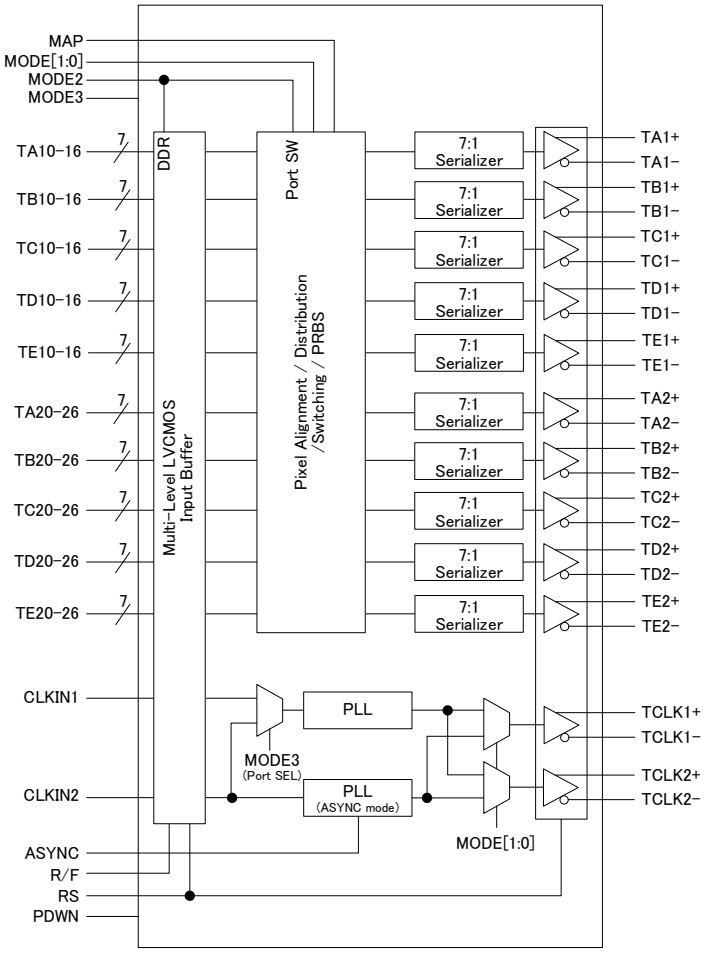


Figure 1. Block Diagram

Pin Diagram

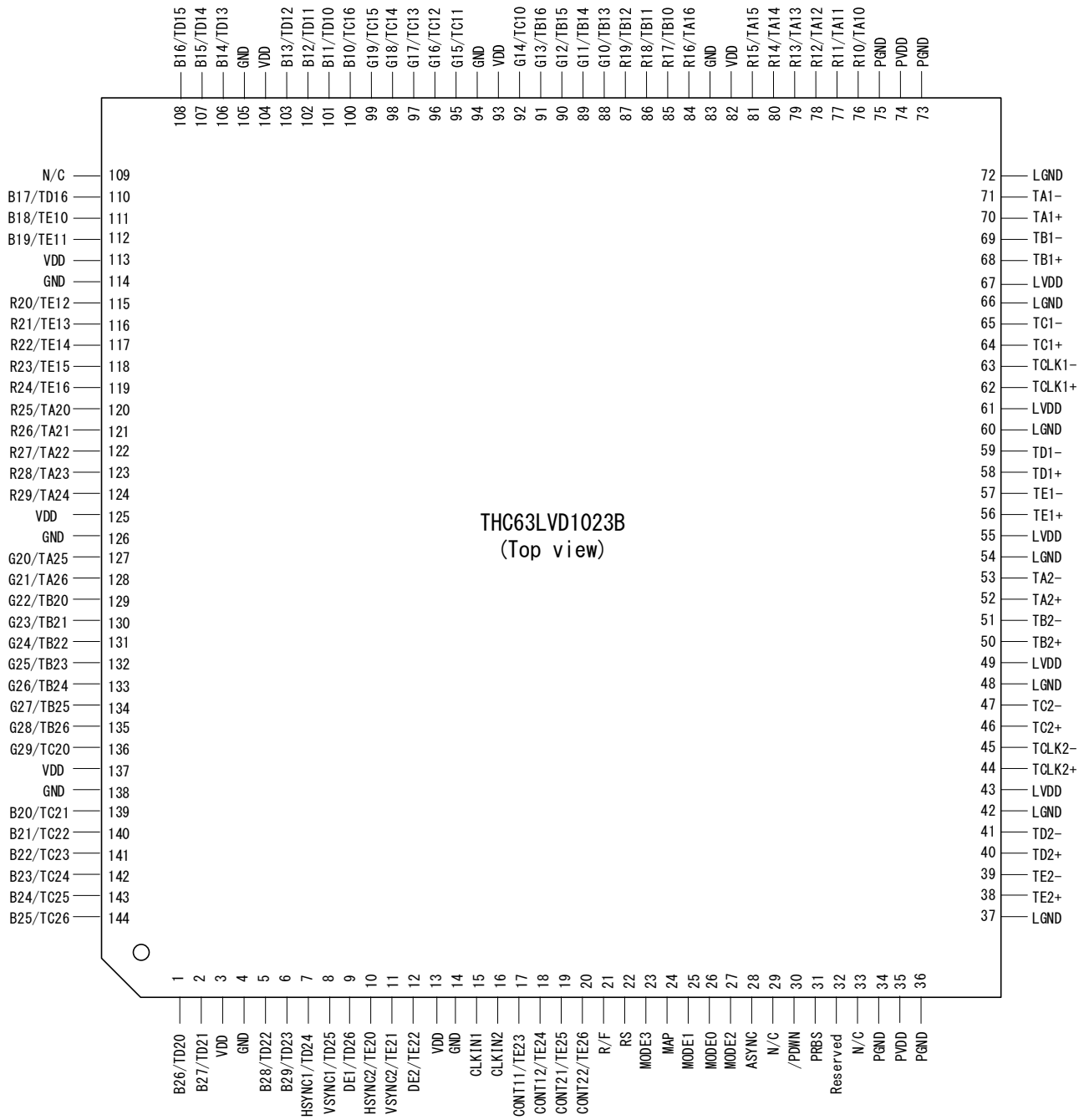


Figure 2. Pin Diagram

Pin Description

Table 1. Pin Description

Pin Name		Type	Description
ASYNC=L	ASYNC=H		
TA1+, TA1- TB1+, TB1- TC1+, TC1- TD1+, TD1- TE1+, TE1-		LVDS Output	Serial Data Output Port 1
TCLK1+,TCLK1-			Port 1 Clock Output
TA2+, TA2- TB2+, TB2- TC2+, TC2- TD2+, TD2- TE2+, TE2-			Serial Data Output Port 2
TCLK2+,TCLK2-			Port 2 Clock Output
R19 - R10 G19 - G10 B19 - B10 DE1 HSYNC1 VSYNC1 CONT11 CONT12	TA16 - TA10 TB16 - TB10 TC16 - TC10 TD16 - TD10 TE16 - TE10	Multi-level LVCMOS Input	Parallel Data Input Port 1
CLKIN1			Port 1 Clock Input
R29 – R20 G29 – G20 B29 – B20 DE2 HSYNC2 VSYNC2 CONT21 CONT22	TA26 – TA20 TB26 – TB20 TC26 - TC20 TD26 - TD20 TE26 - TE20		Parallel Data Input Port 2
CLKIN2			Port 2 Clock Input
RS		3-level LVCMOS Input	ASYNC=H Invalid. Fix to low. ASYNC=L LVCMOS threshold, LVDS swing, V_{REF} voltage control. **See Table 4**.
MAP			ASYNC=H Invalid. Fix to low. ASYNC=L LVDS data mapping select. **See Figure 4, Figure 5, Figure 6.**
MODE1, MODE0		LVCMOS Input	ASYNC=H Invalid. Fix to low. ASYNC=L Pixel and Link configuration mode select. **See Table 2.**
MODE2			ASYNC=H Port swap function enable. **See Table 3** ASYNC=L Distribution and DDR enable. **See Table 2**
MODE3			ASYNC=H Invalid. Fix to low. ASYNC=L Input port select in Single-in/Dual-out mode. **See Table 2**
ASYNC			ASYNC mode enable H : Enable L : Disable (SYNC mode)
R/F			CLKIN1,CLKIN2 triggering edge select H : Rising edge L : Falling edge
/PDWN			Power down mode H : Normal operation L : Power down (all outputs are High-Z.)
PRBS			PRBS pattern generator enable H : PRBS pattern generator enable L : Normal operation
Reserved		-	Must be tied to GND.

Pin Description (Continued)

Pin Name	Type	Description
N/C		Must be open.
VDD	Power	3.3V Digital Circuit and LVCMOS I/O Power Supply
GND	Ground	Digital Circuit and LVCMOS I/O Ground
LVDD	Power	3.3V LVDS Power Supply
LGND	Ground	LVDS Ground
PVDD	Power	3.3V PLL Power Supply
PGND	Ground	PLL Ground

Functional Description

ODD/EVEN pixel alignment and Distribution function in SYNC mode (ASYNC=L)

In SYNC mode, the device operates with one of the clock signals CLKIN1 or CLKIN2, regardless of whether it is a Single port or Dual port input. When using Single-in/Dual-out mode, the DE signal width should be an even multiple of the clock signal input for both High and Low periods, and the same DE signal should be input to DE1 and DE2 (See Figure 12).

Table 2. SYNC mode pin settings

Mode name	Port	Input Pixel Order*	Output Pixel Order	Pin settings					See Figure 4,5,6
				ASYNC	MODE0	MODE1	MODE2	MODE3	
Dual-Link mode	1	1,3…	1,3…	L	L	L	-	-	x=1
	2	2,4…	2,4…						y=2
Single-Link mode	1	1,2,3,4…	1,2,3,4…	L	H	H	L	-	x=1
	2	Unused	Unused						Hi-z
Single-in/Dual-out mode 1	1	1,2,3,4…	1,3…	L	L	H	H/L	H/ Open	x=1
	2	Unused	2,4…						y=1
Single-in/Dual-out mode 2	1	Unused	1,3…	L	L	H	H/L	L	x=2
	2	1,2,3,4…	2,4…						y=2
Dual-in/Single-out mode	1	1,3…	1,2,3,4…	L	H	L	-	-	x=1,2
	2	2,4…	Unused						Hi-z
Distribution mode	1	1,2,3,4…	1,2,3,4…	L	H	H	H	-	x=1
	2	Unused	1,2,3,4…						y=1

*In Single-in/Dual-out mode, the pixel data immediately after the rising edge of the DE signal is the 1st pixel.

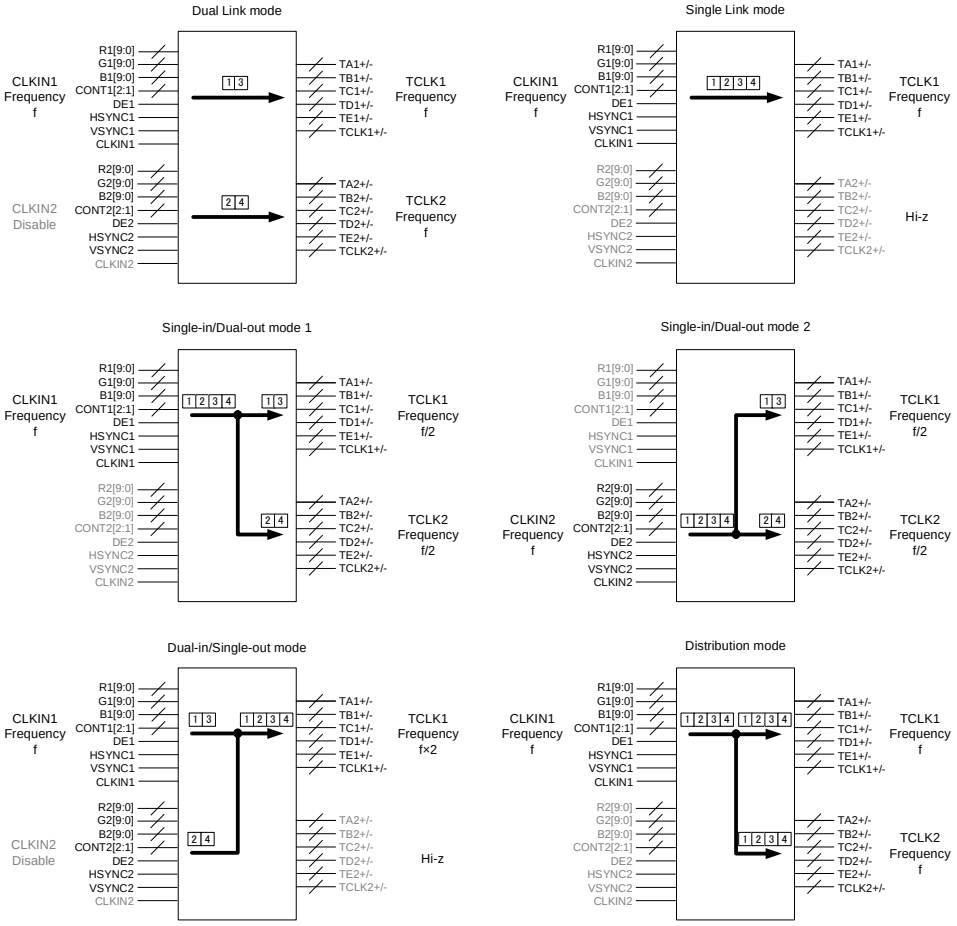
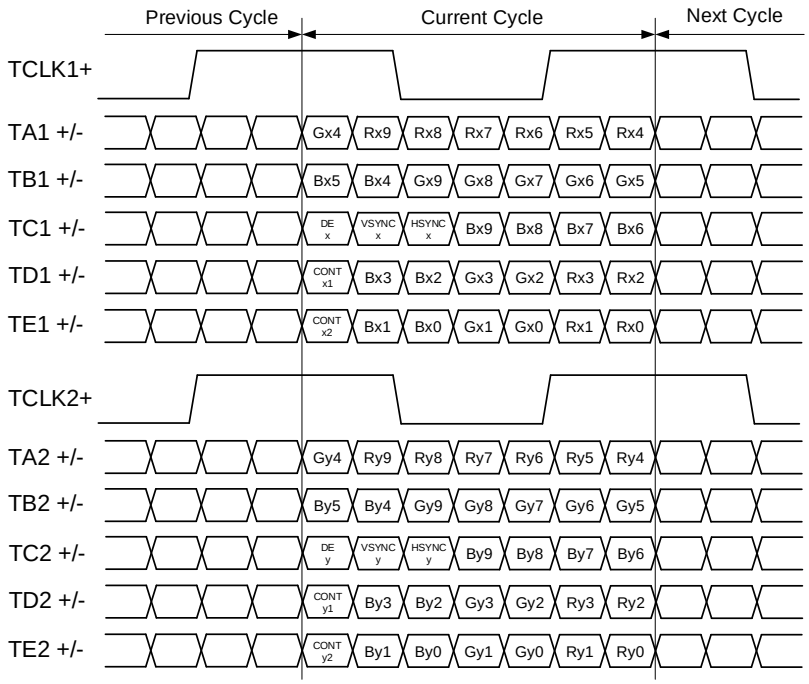
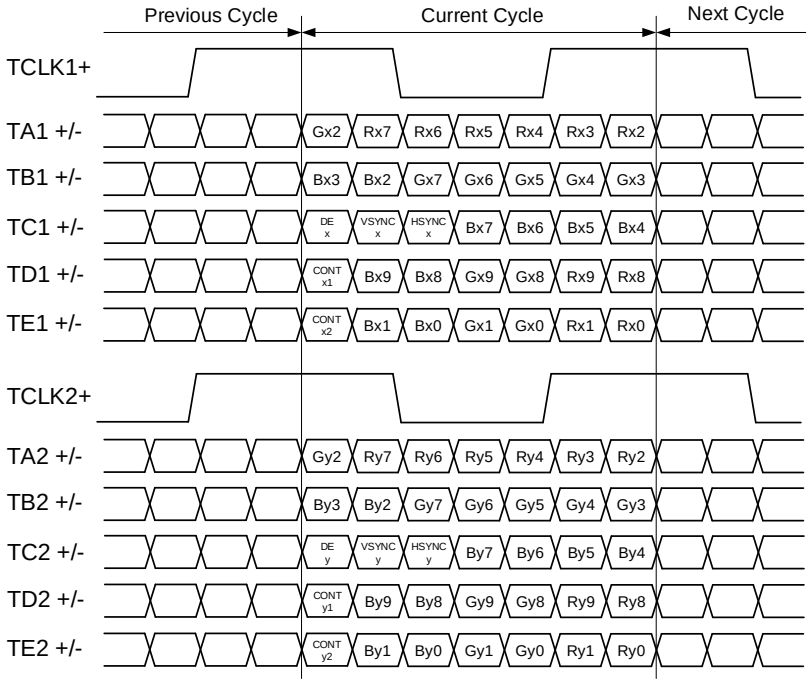


Figure 3. SYNC mode Input and Output signal flow



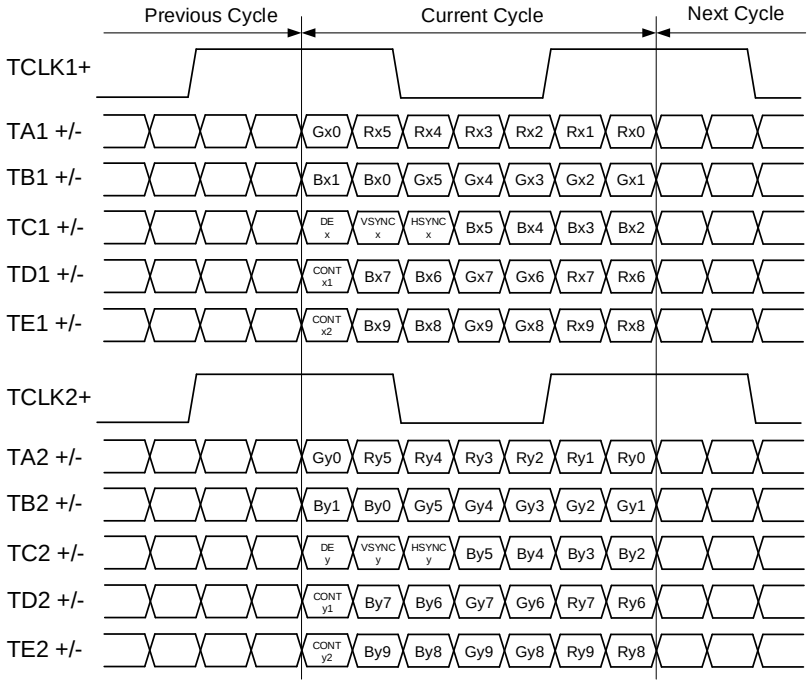
x, y : See the rightmost column of Table 2.

Figure 4. LVCMOS Inputs Mapped to LVDS Outputs (ASYNC=L, MAP=V_{IH3})



x, y : See the rightmost column of Table 2.

Figure 5. LVCMOS Inputs Mapped to LVDS Outputs (ASYNC=L, MAP=V_{IL3})



x, y : See the rightmost column of Table 2.

Figure 6. LVCMOS Inputs Mapped to LVDS Outputs (ASYNC=L, MAP=V_{IM3})

Port switching function in ASYNC mode (ASYNC = H)

ASYNC mode is an asynchronous mode that allows Port1 and Port2 to operate with different clock signals. If only one of the Port1 or Port2 inputs is used, the unused LVDS output Port is Hi-z.

Table 3. ASYNC mode pin settings

Mode name	Port	Input Pixel Order	Output Pixel Order	Pin settings					See Figure 8
				ASYNC	MODE0	MODE1	MODE2	MODE3	
Port SW OFF	1	1,2,3,4…	1,2,3,4…	H	-	-	L	-	x=1
	2	A,B,C,D…	A,B,C,D…						y=2
Port SW ON	1	1,2,3,4…	A,B,C,D…	H	-	-	H	-	x=2
	2	A,B,C,D…	1,2,3,4…						y=1

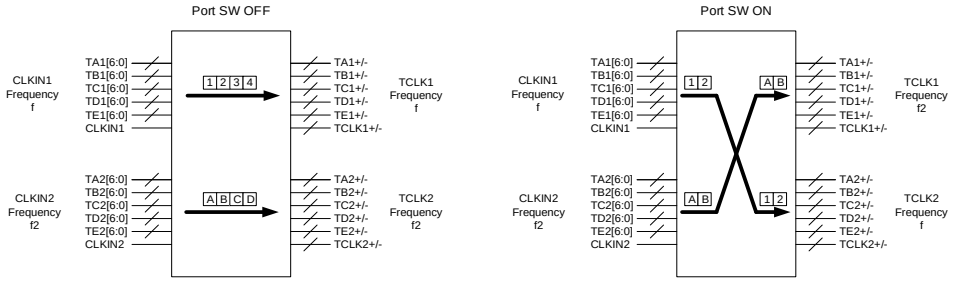
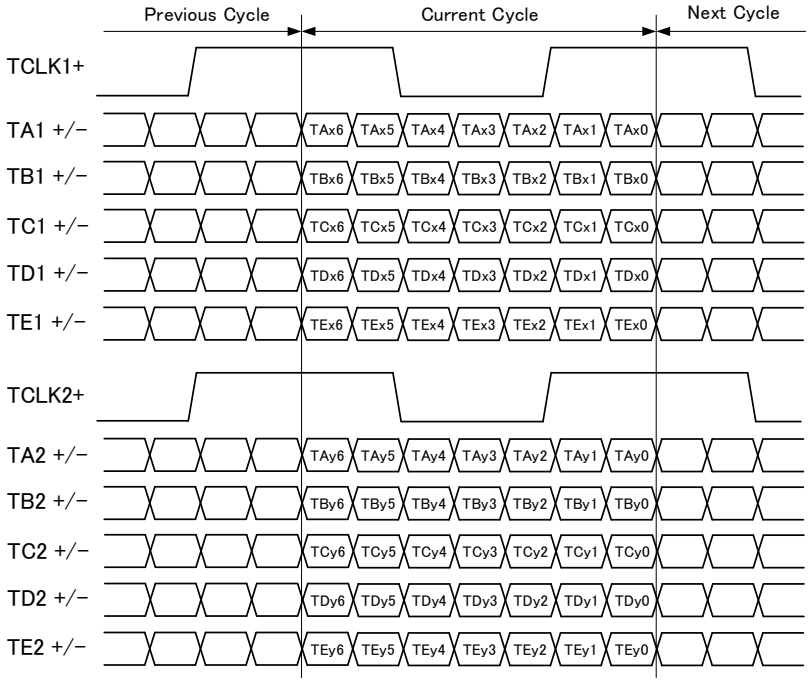


Figure 7. ASYNC mode Input and Output signal flow



x, y : See the rightmost column of Table 3.

Figure 8. LVCMOS Inputs Mapped to LVDS Outputs (ASYNC=H, MAP=Low)

RS pin functions

The voltage applied to the RS pin changes the threshold voltage of the Multi-level LVCMOS input, the LVDS output swing voltage, and the V_{REF} voltage.

Table 4. RS pin settings

RS pin voltage	Multi-level LVCMOS Input threshold voltage (V_{IHM}, V_{ILM})	LVDS Output Swing voltage (VOD)	V_{REF} voltage
V_{IH3}	V_{ILM}<0.8V, V_{IHM}>2.0V	Typ.350mV	VDD/2
V_{IM3}	V_{IHM}>RS+0.1V , V_{ILM}<RS-0.1V	Typ.350mV	RS pin Voltage
V_{IL3}	V_{ILM}<0.8V, V_{IHM}>2.0V	Typ.200mV	VDD/2

Pseudo-Random Binary Sequence (PRBS) pattern generator

It has a PRBS pattern generator that can be used in Dual-in/Dual-out and ASYNC modes. The PRBS pattern signal is "2^{23}-1". This signal is serialized and output as an LVDS signal.

Absolute Maximum Ratings

Table 5. Absolute Maximum Rating

Parameter	Min	Max	Unit
Power Supply Voltage	-0.3	+4.0	V
LVCMOS Input Voltage	-0.3	VDD + 0.3	V
LVDS Output Voltage	-0.3	VDD + 0.3	V
Output Current	-30	+30	mA
Junction Temperature	-	+125	°C
Storage Temperature	-55	+125	°C
Reflow Peak Temperature	-	+260	°C
Reflow Peak Temperature Time	-	10	sec
Maximum Power Dissipation @+25°C	-	2.4	W

"Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. They are not meant to imply that the device should be operated at these limits. "Absolute Maximum Rating" value also includes behavior of overshooting and undershooting.

Recommended Operating Conditions

Table 6. Recommended Operating Conditions

Symbol	Parameter				Min	Typ	Max	Unit
VDD33	All Supply Voltage (VDD, LVDD, PVDD)				3.0	3.3	3.6	V
Ta	Operating Ambient Temperature				-20	-	70	°C
PCLK	Clock Frequency	MODE<1:0>=L:L (Dual-in/Dual-out)		CLKIN	20	-	160	MHz
				TCLK	20	-	160	
		MODE<1:0>=L:H (Dual-in/Single-out)		CLKIN	10	-	80	
				TCLK	20	-	160	
		MODE<1:0>=H:L (Single-in/Dual-out)	MODE2=L DDR : Disable	CLKIN	40	-	160	
				TCLK	20	-	80	
			MODE2=H DDR : Enable	CLKIN	20	-	80	
				TCLK	20	-	80	
		MODE<1:0>=H:H (Single-in/Single-out)		CLKIN	20	-	160	
				TCLK	20	-	160	
		ASYNC=H (Dual-in/Dual-out, Asynchronous mode)		CLKIN	20	-	160	
				TCLK	20	-	160	

Power Consumption

Table 7. Supply Current

Symbol	Parameter	Conditions			Max	Unit
I_{TCCW}	Operating Current	RL=100Ω CL=5pF RS=VDD Test Signal Pattern (Figure 9.)	Single Link mode	CLKIN=65MHz	105	mA
				CLKIN=85MHz	121	mA
				CLKIN=135MHz	157	mA
				CLKIN=160MHz	179	mA
			Distribution mode	CLKIN=65MHz	146	mA
				CLKIN=85MHz	172	mA
				CLKIN=135MHz	217	mA
				CLKIN=160MHz	250	mA
			Single-in/Dual-out mode (DDR Input ON)	CLKIN=65MHz	108	mA
				CLKIN=85MHz	136	mA
				CLKIN=135MHz	169	mA
				CLKIN=160MHz	194	mA
			Single-in/Dual-out mode (DDR Input OFF)	CLKIN=32.5MHz	120	mA
				CLKIN=42.5MHz	140	mA
				CLKIN=67.5MHz	183	mA
				CLKIN=80MHz	199	mA
			Dual-in/Single-out mode	CLKIN=32.5MHz	95	mA
				CLKIN=42.5MHz	110	mA
				CLKIN=67.5MHz	143	mA
				CLKIN=80MHz	166	mA
			Dual Link mode	CLKIN=65MHz	167	mA
				CLKIN=85MHz	197	mA
				CLKIN=135MHz	261	mA
				CLKIN=160MHz	301	mA
			ASYNC mode	CLKIN=65MHz	183	mA
				CLKIN=85MHz	214	mA
				CLKIN=135MHz	286	mA
				CLKIN=160MHz	329	mA
	Power Down Current	/PDWN=L, All Inputs=Fixed L or H			50	uA

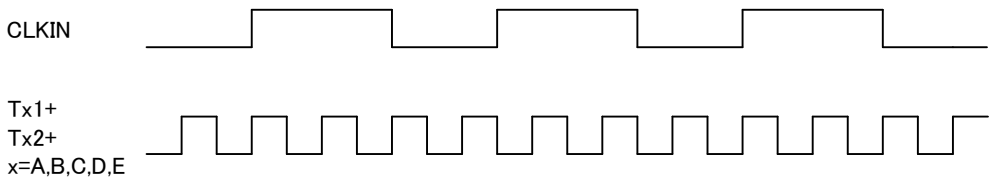


Figure 9. Test Signal Pattern

Electrical Characteristics

DC Specifications

Table 8. DC Specifications

Symbol	Parameter	Conditions	Min	Typ*	Max	Unit
LVCMOS DC Specifications						
V_{IHM}	Multi-level LVCMOS Input High Level Voltage	RS=V_{IH3} or V_{IL3}	2.0	-	VDD	V
		RS=V_{IM3}	RS +0.1	-	-	V
V_{ILM}	Multi-level LVCMOS Input Low Level Voltage	RS=V_{IH3} or V_{IL3}	GND	-	0.8	V
		RS= V_{IM3}	-	-	RS -0.1	V
V_{IH}	LVCMOS Input High Level Voltage		2.0	-	VDD	V
V_{IL}	LVCMOS Input Low Level Voltage		GND	-	0.8	V
V_{IH3}	3-level Input High Level Voltage		0.8 ×VDD	-	VDD	V
V_{IM3}	3-level Input Middle Level Voltage		0.6	-	1.4	V
V_{IL3}	3-level Input Low Level Voltage		GND	-	0.08 ×VDD	V
I_{INC}	Input Current	Except MODE3 pin, V_{IN}=GND~VDD	-	-	±10	uA
I_{INCM3}	MODE3 pin Input Current	V_{IN}=GND~VDD	-	-	±20	uA
LVDS DC Specifications						
VOD	Differential Output Voltage	RL=100Ω, RS=V_{IH3} or V_{IM3}	250	350	450	mV
		RL=100Ω, RS=V_{IL3}	100	200	300	mV
ΔVOD	Change in VOD between complementary output states	RL=100Ω	-	-	35	mV
VOC	Common Mode Voltage	RL=100Ω	1.125	1.25	1.375	V
ΔVOC	Change in VOC between complementary output states	RL=100Ω	-	-	35	mV
I_{OS}	Output Short Circuit Current	V_{OUT}=GND, RL=100Ω	-	-	-24	mA
I_{OZ}	Output Tri-State Current	/PDWN=GND, VOUT=GND~VDD	-	-	±10	uA

* Typ values are at the conditions of VDD=LVDD=PVDD=3.3V and Ta = +25ºC

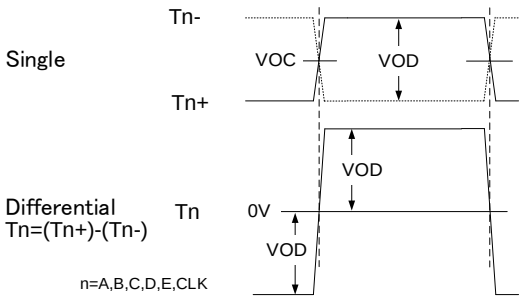


Figure 10. LVDS Common mode and Differential Voltage

Switching Characteristics

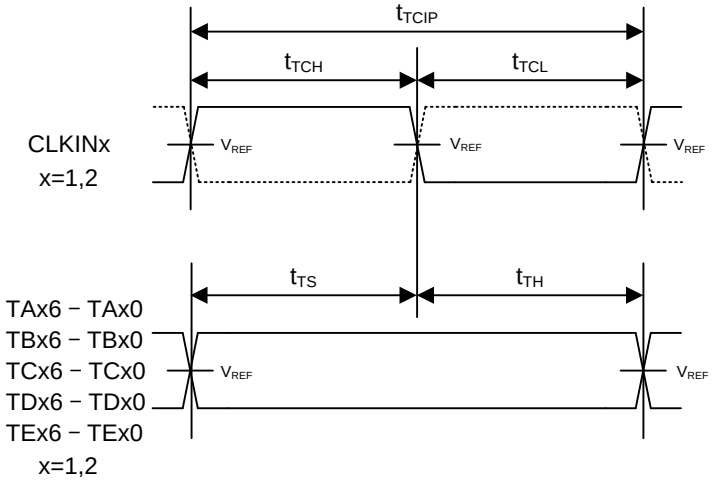
Table 9. AC Specifications

Symbol	Parameters	Conditions	Min	Typ*	Max	Units
LVCMOS AC Specifications						
t_{TCIP}	CLKIN Period		6.25	-	100	ns
t_{TCH}	CLKIN High Time		0.35×t_{TCIP}	0.5×t_{TCIP}	0.65×t_{TCIP}	ns
t_{RCL}	CLKIN Low Time		0.35×t_{TCIP}	0.5×t_{TCIP}	0.65×t_{TCIP}	ns
t_{TS}	Data Setup time to CLKIN		2.5	-	-	ns
t_{TH}	Data Hold time to CLKIN		0	-	-	ns
t_{TCD}	CLKIN to TCLK Delay	MODE<1:0>=L:L (Dual-in/Dual-out, ASYNC)	(4+3/7) ×t_{TCIP}+2.6	-	(4+3/7) ×t_{TCIP}+7.5	ns
LVDS AC Specifications						
t_{TCOP}	TCLK Period		6.25	-	50	ns
t_{LVT}	LVDS Output Transition Time	t_{TCOP}=6.25ns~20ns	-	0.6	1.5	ns
t_{TOP1}	Output Data Position1	t_{TCOP}=6.25ns~20ns	-0.15	0.0	+0.15	ns
t_{TOP0}	Output Data Position 0	t_{TCOP}=6.25ns~20ns	t_{TCOP}/7 - 0.15	t_{TCOP}/7	t_{TCOP}/7 + 0.15	ns
t_{TOP6}	Output Data Position6	t_{TCOP}=6.25ns~20ns	2×t_{TCOP}/7 - 0.15	2×t_{TCOP}/7	2×t_{TCOP}/7 + 0.15	ns
t_{TOP5}	Output Data Position5	t_{TCOP}=6.25ns~20ns	3×t_{TCOP}/7 - 0.15	3×t_{TCOP}/7	3×t_{TCOP}/7 + 0.15	ns
t_{TOP4}	Output Data Position4	t_{TCOP}=6.25ns~20ns	4×t_{TCOP}/7 - 0.15	4×t_{TCOP}/7	4×t_{TCOP}/7 + 0.15	ns
t_{TOP3}	Output Data Position3	t_{TCOP}=6.25ns~20ns	5×t_{TCOP}/7 - 0.15	5×t_{TCOP}/7	5×t_{TCOP}/7 + 0.15	ns
t_{TOP2}	Output Data Position2	t_{TCOP}=6.25ns~20ns	6×t_{TCOP}/7 - 0.15	6t_{TCOP}/7	6×t_{TCOP}/7 + 0.15	ns
Delay time						
t_{TPLL}	PLL Lock Time		-	-	10	ms
t_{TPD}	Power On to /PDWN High		0	-	-	ns
DE Input Timing						
t_{DEINT}	DE Input Period	MODE<2:1:0>=L:H:L (Single-in/Dual-out, DDR Input mode Disable), n="integer"	4×t_{TCIP}	2n×t_{TCIP}	-	ns
t_{DEH}	DE High Time	MODE<2:1:0>=L:H:L (Single-in/Dual-out, DDR Input mode Disable), m="integer"	2×t_{TCIP}	2m×t_{TCIP}	-	ns
t_{DEINT}	DE Low Time	MODE<2:1:0>=L:H:L (Single-in/Dual-out, DDR Input mode Disable)	2×t_{TCIP}	-	-	ns

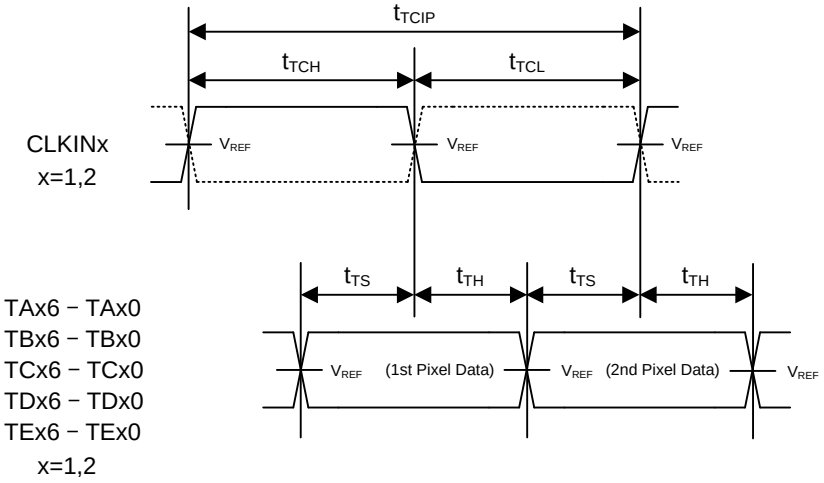
* Typ values are at the conditions of VDD=LVDD=PVDD=3.3V and Ta = +25ºC

Multi-level LVCMOS Input

Normal mode



DDR mode

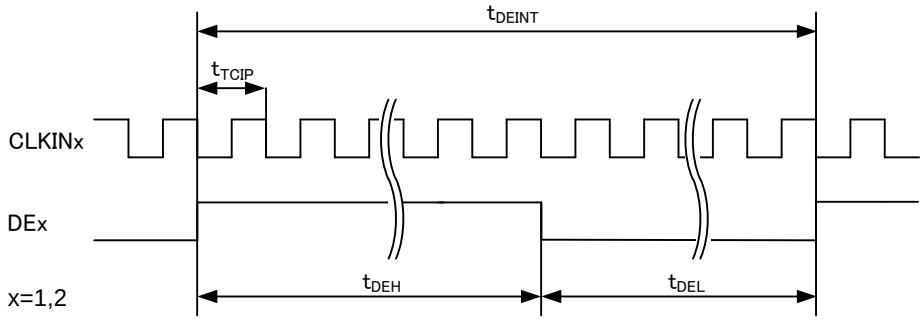


Note: CLKIN signal notation

R/F = GND : Solid line
R/F = VDD : Dash line

Figure 11. LVCMOS Input Setup and Hold Time

Data Enable (DE) signal input timing requirement



Note: Single-in/Dual-out, DDR off mode (MODE<2:1:0>=L:H:L)

In this case, MUST input Data Enable Signal (DE1/DE2pin).
The period between rising edges of DE (t_{DEINT}), high time of DE (t_{DEH}) should always satisfy following equations.

$$t_{DEH} = t_{TCIP} \times (2m)$$

$$t_{DEINT} = t_{TCIP} \times (2n)$$

m, n = integer

Figure 12. DE signal input timing requirement

LVDS Output

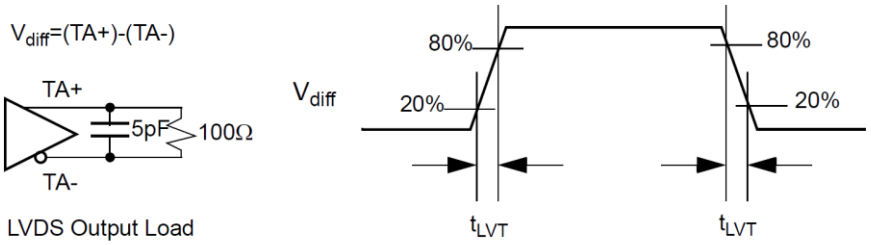


Figure 13. LVDS Output Load and Transition Time

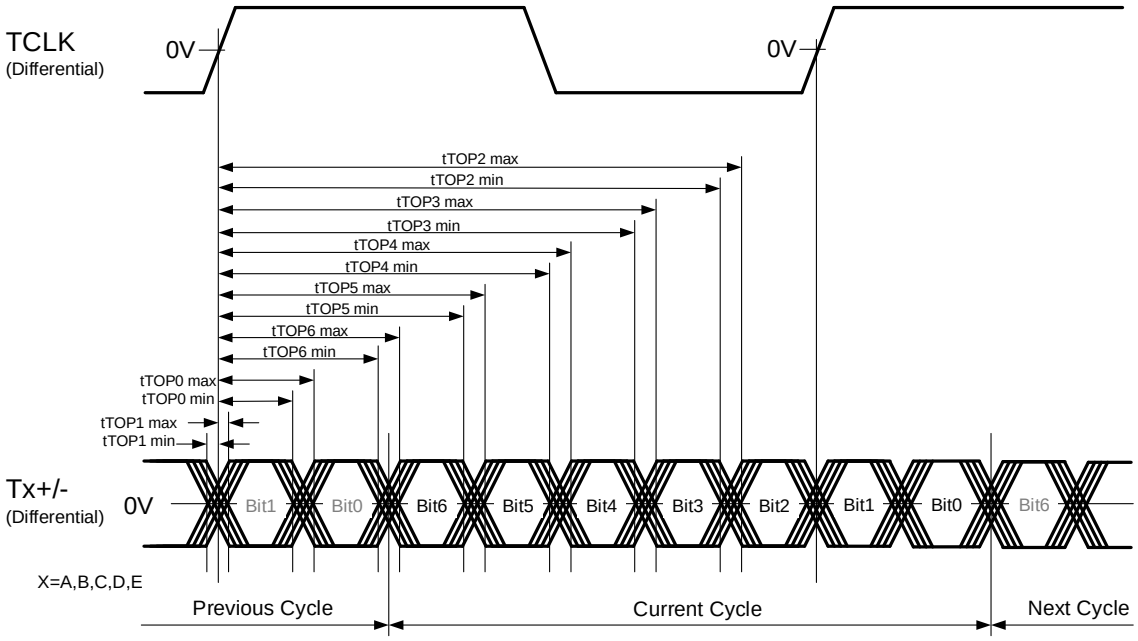
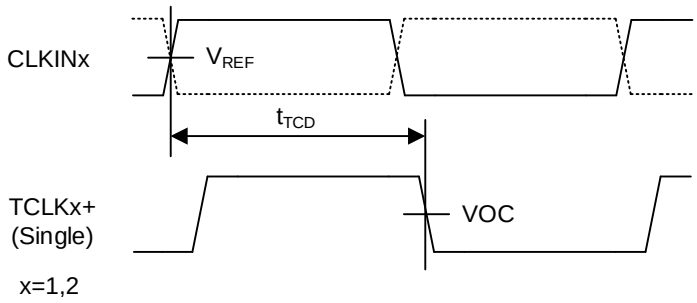


Figure 14. LVDS Output Data Position

Input to Output Delay

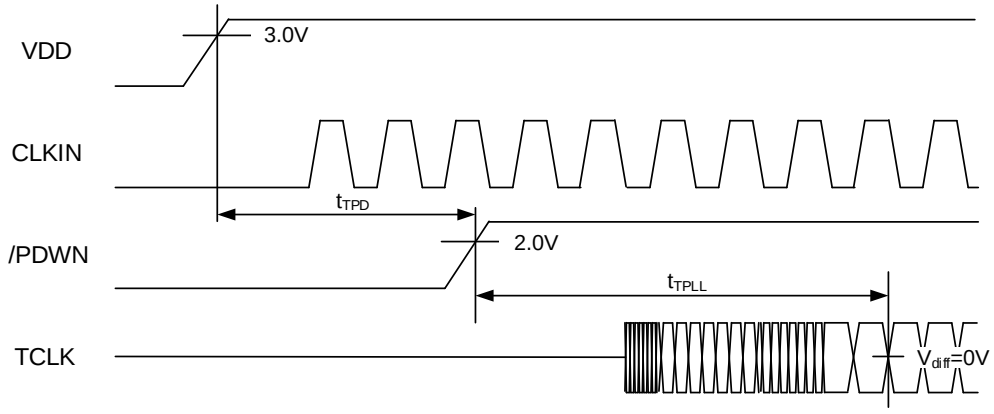


Note: CLKIN signal notation
R/F = GND : Solid line
R/F = VDD : Dash line

Figure 15. Input Clock to Output Clock Delay Time

Power on Sequence

/PDWN Control after CLKIN Input



CLKIN Input after /PDWN Control

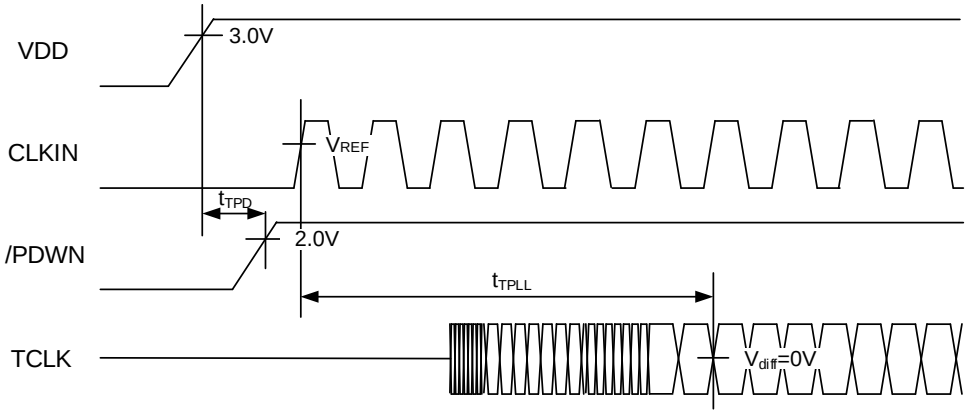


Figure 16. Power on Sequence

Notes

1) Cable Connection and Disconnection

Do not connect and disconnect the LVDS cable, when the power is supplied to the system.

2) GND Connection

Connect each GND of the PCB which THC63LVD1023B and LVDS-Rx on it. It is better for EMI reduction to place GND cable as close to LVDS cable as possible.

3) Multi Drop Connection

Multi drop connection is not recommended.

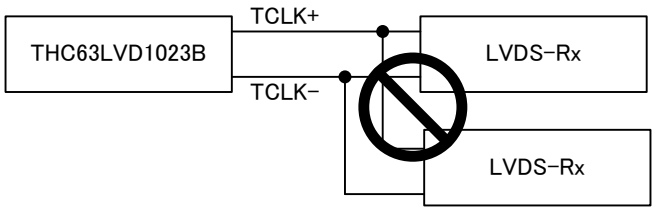


Figure 17. Multi Drop Connection

4) Asynchronous use

Asynchronous using such as following system is not recommended.

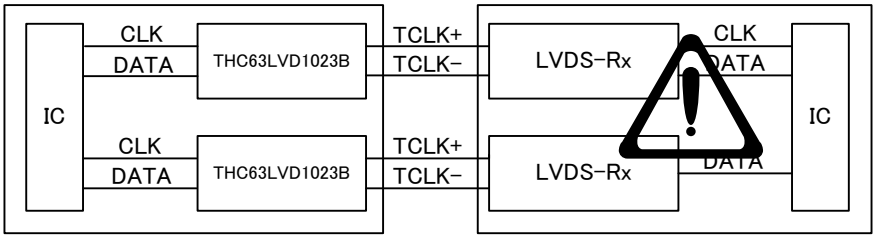


Figure 18. Asynchronous Use

Package

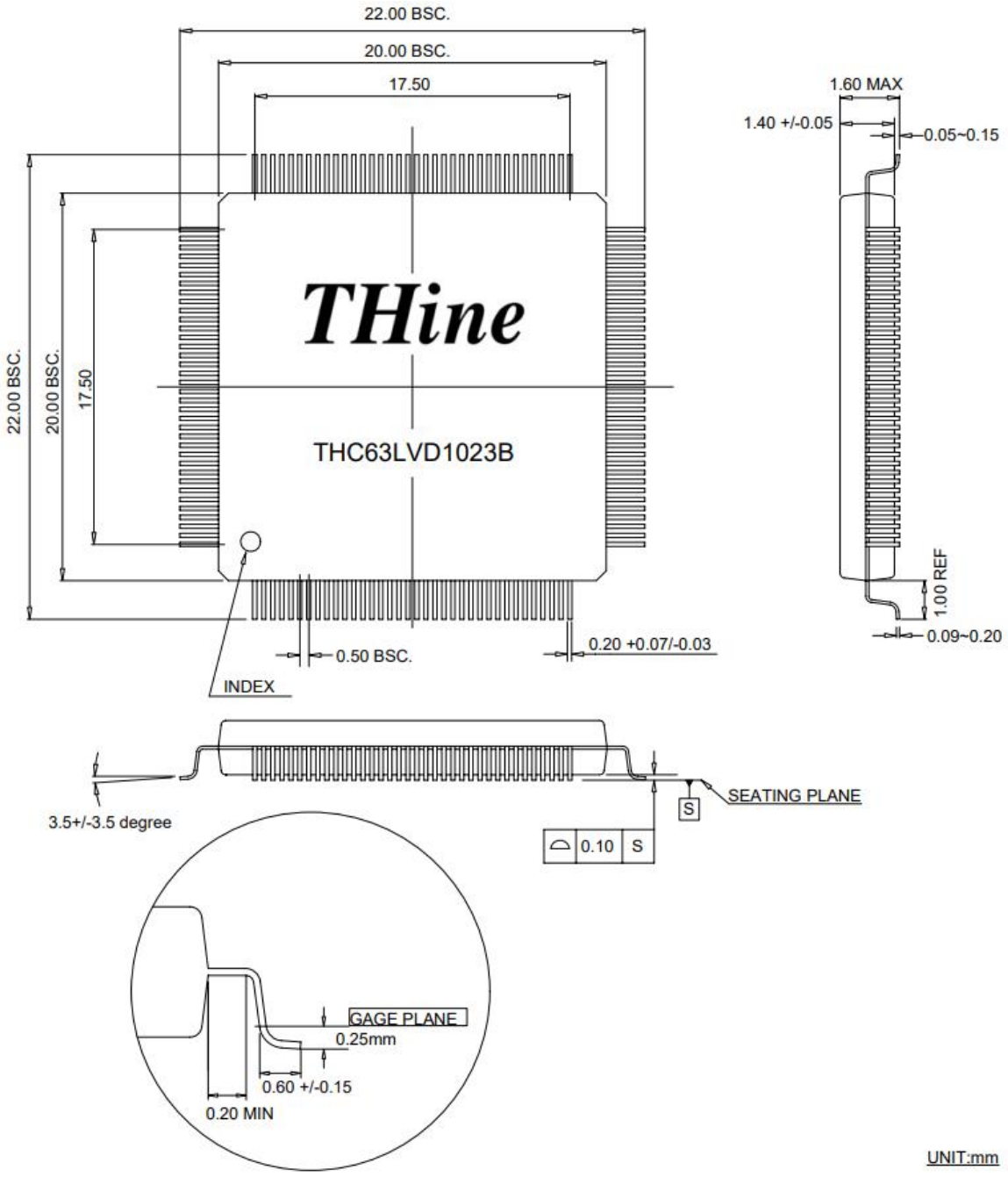


Figure 19. Package Diagram

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