THC63LVD1027D

Dual Link LVDS Repeater

General Description

The THC63LVD1027D LVDS(Low Voltage Differential Signaling) repeater is designed to support pixel data transmission between Host and Flat Panel Display up to WUXGA resolution.
THC63LVD1027D receives the dual link LVDS data streams and transmits the LVDS data through various line rate conversion modes, Dual Link Input / Dual Link Output, Single Link Input / Dual Link Output, and Dual Link Input / Single Link Output.

Features

- 30bits/pixel dual link LVDS Receiver
- 30bits/pixel dual Link LVDS Transmitter
- Operating Temperature Range : -40ºC~105ºC (*)
- Wide LVDS input skew margin: ± 480ps at 85MHz
- Accurate LVDS output timing: ± 250ps at 85MHz
- Reduced swing LVDS output mode supported to suppress the system EMI
- Various line rate conversion modes supported

Dual link input / Dual link output [clkout=1x clkin]
Single link input / Dual link output [clkout=1/2x clkin]
Dual link input / Single link output [clkout=2x clkin]

- Distribution (signal duplication) mode supported
- Power down mode supported
- 3.3V single voltage power supply
- 64pin TSSOP with Exposed PAD (0.5mm lead pitch)

(*) Refer to Fig.1 Block Diagram

Block Diagram

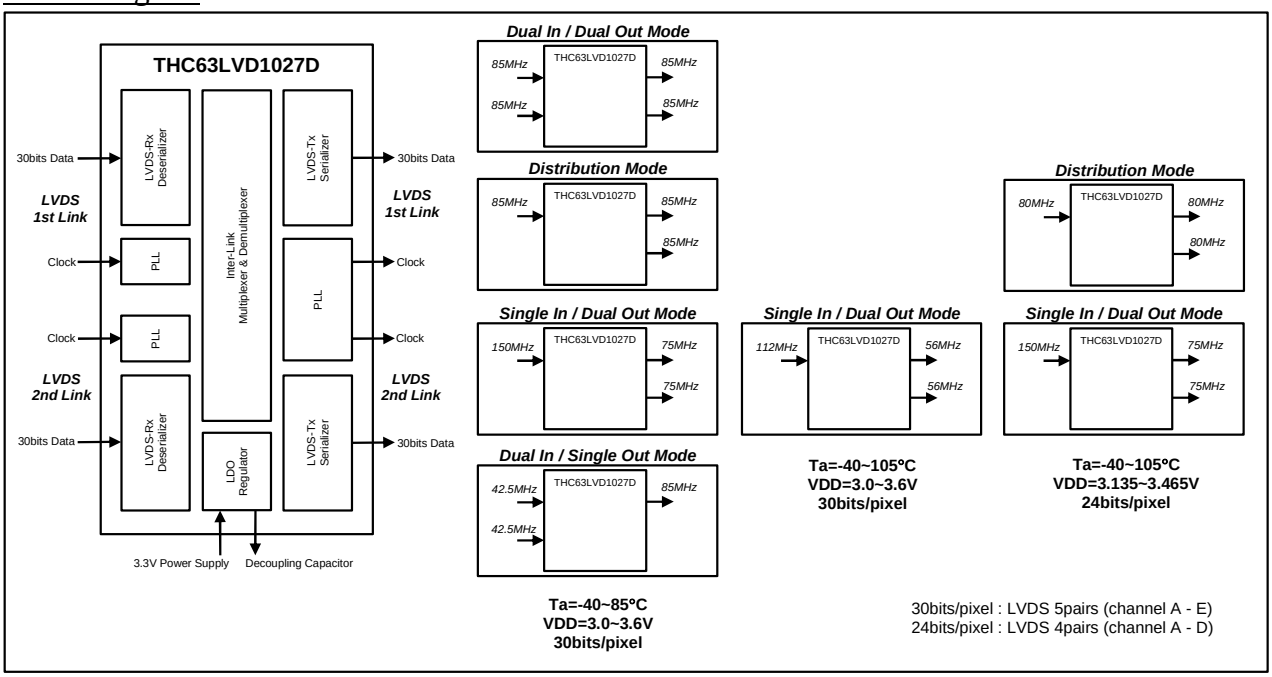


Fig.1 Block Diagram

Pin Diagram

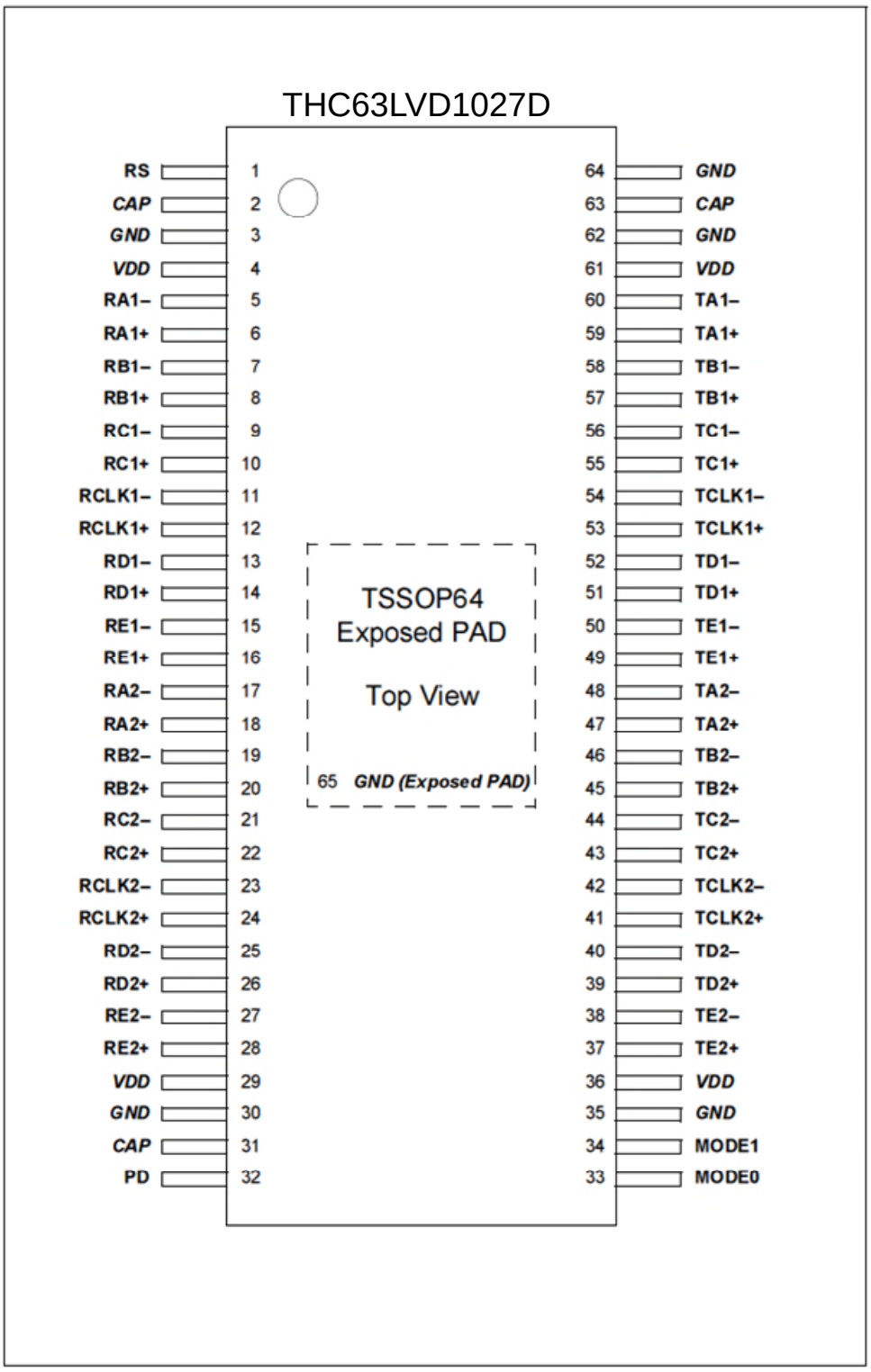


Fig.2 Pin Diagram

Pin Description

Table 1. Pin Description

Pin Name	Pin #	Direction	Type	Description
RA1+/-	6, 5	Input	LVDS	**LVDS data input for channel A of 1st Link**
RB1+/-	8, 7			**LVDS data input for channel B of 1st Link**
RC1+/-	10, 9			**LVDS data input for channel C of 1st Link**
RD1+/-	14, 13			**LVDS data input for channel D of 1st Link**
RE1+/-	16, 15			**LVDS data input for channel E of 1st Link**
RCLK1+/-	12, 11			**LVDS clock input for 1st Link**
RA2+/-	18, 17			**LVDS data input for channel A of 2nd Link**
RB2+/-	20, 19			**LVDS data input for channel B of 2nd Link**
RC2+/-	22, 21			**LVDS data input for channel C of 2nd Link**
RD2+/-	26, 25			**LVDS data input for channel D of 2nd Link**
RE2+/-	28, 27			**LVDS data input for channel E of 2nd Link**
RCLK2+/-	24, 23			**LVDS clock input for 2nd Link** In Distribution and Single-in/Dual-out mode,RCLK2+/- must be Hi-Z. (See "Mode selection" below in this page.)
TA1+/-	59, 60	Output		**LVDS data output for channel A of 1st Link**
TB1+/-	57, 58			**LVDS data output for channel B of 1st Link**
TC1+/-	55, 56			**LVDS data output for channel C of 1st Link**
TD1+/-	51, 52			**LVDS data output for channel D of 1st Link**
TE1+/-	49, 50			**LVDS data output for channel E of 1st Link**
TCLK1+/-	53, 54			**LVDS clock output for 1st Link**
TA2+/-	47, 48			**LVDS data output for channel A of 2nd Link**
TB2+/-	45, 46			**LVDS data output for channel B of 2nd Link**
TC2+/-	43, 44			**LVDS data output for channel C of 2nd Link**
TD2+/-	39, 40			**LVDS data output for channel D of 2nd Link**
TE2+/-	37, 38			**LVDS data output for channel E of 2nd Link**
TCLK2+/-	41, 42			**LVDS clock output for 2nd Link**
PD	32	Input	LVCMOS	**Power Down** H: Normal operation L: Power down state, all LVDS output signals turn to Hi-Z
RS	1			**LVDS output swing level selection** H: Normal swing L: Reduced swing
MODE1 **MODE0**	34 33			**Mode selection** MODE1 / MODE0 / RCLK2+/- / Description L / L / CLKIN / Dual-in/Dual-out mode L / L / Hi-Z / Distribution mode H / L / Hi-Z / Single-in/Dual-out mode L / H / CLKIN / Dual-in/Single-out mode H / H / - / Reserved In Distribution and Single-in/Dual-out mode, RCLK2+/- must be Hi-Z.
VDD	4, 29, 36, 61	Power	-	**3.3V power supply pins**
GND	3, 30, 35, 62, 64, 65			**Ground pins (Exposed PAD is also Ground)**
CAP	2, 31, 63			**Decoupling capacitor pins** These pins should be connected to external decoupling capacitors (Ccap). Recommended Ccap is 0.1μF.

Mode Setting

Table 2. Mode Setting

Input/Output	RCLK2+/-	MODE1 (Input mode)	MODE0 (Output mode)
		H: Single L: Dual	H: Single L: Dual
Dual-In/Dual-Out (Fig.3-1,12-1)	CLKIN	L	L
Distribution (Fig.3-2,12-2)	Hi-Z	L	L
Single-In/Dual-Out (Fig.3-3,12-3)	Hi-Z	H	L
Dual-In/Single-Out (Fig.3-4,12-4)	CLKIN	L	H
Reserved	-	H	H

Signal Flow for Each Setting

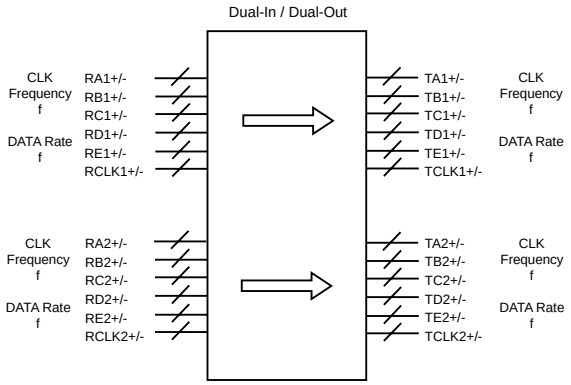


Fig.3-1

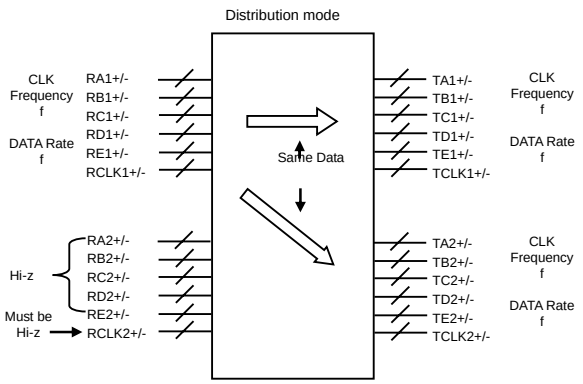


Fig.3-2

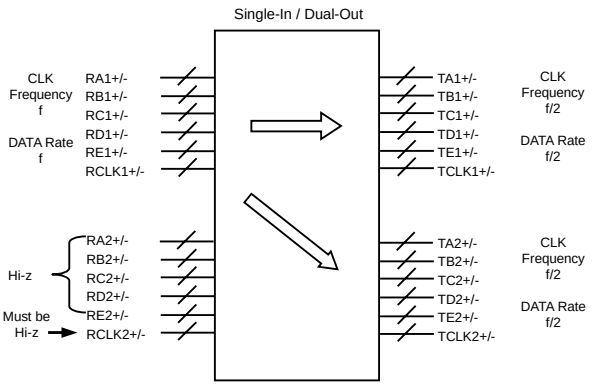


Fig.3-3

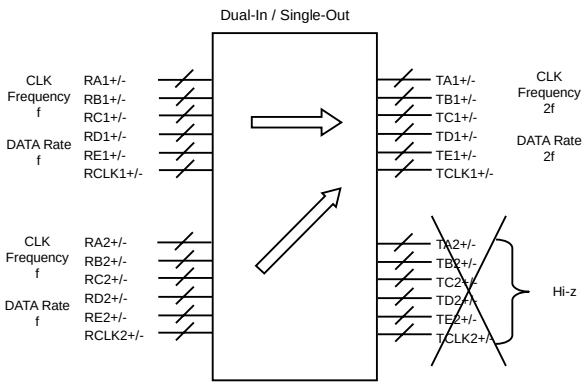


Fig.3-4

Output Control / Fail Safe

THC63LVD1027D has a function to control output depending on LVDS input condition.

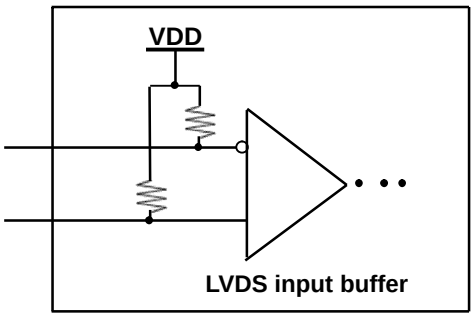
Table 3. Output Control

PD	RCLK1+/-	RCLK2+/-	Output
L	*	*	All Hi-Z
H	Hi-Z	*	All Hi-Z
H	CLKIN	CLKIN	Refer to p.4 Mode Setting #
H	CLKIN	Hi-Z	Refer to p.4 Mode Setting #

*: Don't care

#: If a particular input data pair is Hi-Z, the corresponding output data become L according to LVDS DC spec.

For fail-safe purpose, all LVDS input pins are connected to VDD via resistance for detecting Hi-Z state.



Internal circuit of THC63LVD1027D

Fig.4 Fail Safe Circuit

Absolute Maximum Ratings

Table 4. Absolute Maximum Rating

Parameter	Min	Max	Unit
Power Supply Voltage	-0.3	+4.0	V
LVCMOS Input Voltage	-0.3	V_{DD}+0.3	V
LVDS Input Voltage	-0.3	V_{DD}+0.3	V
Junction Temperature	-	+125	°C
Storage Temperature	-55	+125	°C
Reflow Peak Temperature / Time	-	+260 / 10sec	°C
Maximum Power Dissipation @+25°C	-	2.5	W

ESD Ratings

Table 5. ESD Rating

Parameter	Min	Max	Unit
Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001	-	±8000	V
Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002	-	±1500	V

Operating Conditions

Table 6. Operating Condition

Ta=-40~85°C (30bits/pixel)

Symbol	Parameter		Min	Typ	Max	Unit
T_a	Operating Ambient Temperature		-40	25	85	°C
V_{DD}	Power Supply Voltage		3.0	3.3	3.6	V
f_{CLK}	Dual-In/Dual-Out	CLKIN	20	-	85	MHz
		CLKOUT	20	-	85	
	Distribution	CLKIN	20	-	85	MHz
		CLKOUT	20	-	85	
	Single-In/Dual-Out	CLKIN	40	-	150	MHz
		CLKOUT	20	-	75	
	Dual-In/Single-Out	CLKIN	20	-	42.5	MHz
		CLKOUT	40	-	85	

Ta=-40~105°C (30bits/pixel)

Symbol	Parameter		Min	Typ	Max	Unit
T_a	Operating Ambient Temperature		-40	25	105	°C
V_{DD}	Power Supply Voltage		3.0	3.3	3.6	V
f_{CLK}	Single-In/Dual-Out	CLKIN	40	-	112	MHz
		CLKOUT	20	-	56	

Ta=-40~105°C (24bits/pixel)

Symbol	Parameter		Min	Typ	Max	Unit
T_a	Operating Ambient Temperature		-40	25	105	°C
V_{DD}	Power Supply Voltage		3.135	3.3	3.465	V
f_{CLK}	Distribution	CLKIN	20	-	80	MHz
		CLKOUT	20	-	80	
	Single-In/Dual-Out	CLKIN	40	-	150	MHz
		CLKOUT	20	-	75	

Power Consumption

Table 7. Max Power Consumption

Symbol	Parameter	Conditions (RS=VDD, PRBS pattern)		Ta=-40~85°C VDD=3.0~3.6V 30bits/pixel	Ta=-40~105°C VDD=3.0~3.6V 30bits/pixel	Ta=-40~105°C VDD=3.135~3.465V 24bits/pixel
I_{CCW}	Operating Current	Dual-In/Dual-Out	CLKIN=40MHz	225	N/A	N/A
			CLKIN=65MHz	250		
			CLKIN=75MHz	260		
			CLKIN=85MHz	270		
		Distribution	CLKIN=40MHz	170		160
			CLKIN=65MHz	190		180
			CLKIN=75MHz	200		190
			CLKIN=80MHz	205		195
			CLKIN=85MHz	210		N/A
		Single-In/Dual-Out	CLKIN=40MHz	150	150	145
			CLKIN=65MHz	165	165	155
			CLKIN=75MHz	170	170	160
			CLKIN=85MHz	175	175	165
			CLKIN=112MHz	190	190	180
			CLKIN=135MHz	205	N/A	190
			CLKIN=150MHz	215		195
		Dual-In/Single-Out	CLKIN=20MHz	180		N/A
			CLKIN=32.5MHz	200		
			CLKIN=37.5MHz	210		
			CLKIN=42.5MHz	220		
I_{CCS}	Power Down Current	-	-	8		

（unit ： mA）

Electrical Characteristics

DC Specifications

Table 8. DC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CAP}	Capacitor pin appearance voltage	C_{CAP}=0.1μF	-	1.8	-	V
V_{IH}	High Level Input Voltage	-	2.0	-	VDD	V
V_{IL}	Low Level Input Voltage	-	GND	-	0.8	V
I_{IN_TTL}	LV-TTL Input Leakage Current	-	-4	-	+4	μA

LVDS Receiver DC Specifications

Table 9. LVDS Receiver DC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN_RX}	LVDS-Rx Input Voltage Range	-	0.3	-	2.1	V
V_{IC_RX}	LVDS-Rx Common Voltage	-	0.6	1.2	1.8	
V_{TH_RX}	LVDS-Rx Differential High Threshold	V_{IC_RX} = 1.2V	-	-	+100	mV
V_{TL_RX}	LVDS-Rx Differential Low Threshold		-100	-	-	
$\|V_{ID\_RX}\|$	LVDS-Rx Differential Input Voltage	-	100	-	600	
I_{IN_RX}	LVDS-Rx Input Leakage Current	PD=VDD	-0.3	-	+0.3	mA
		PD=GND Vin=GND or VDD	-10	-	+10	μA

LVDS Transmitter DC Specifications

Table 10. LVDS Transmitter DC Specifications

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{OC_TX}	LVDS-Tx Common Voltage	R_{L_TX} = 100Ω	-	1.125	1.25	1.375	V
ΔV_{OC_TX}	Change in VOC between complementary output states		-	-	-	35	mV
$\|V_{OD\_TX}\|$	LVDS-Tx Differential Output Threshold		Normal Swing	250	350	450	mV
			Reduced Swing	120	200	300	
ΔV_{OD_TX}	Change in VOD between complementary output states		-	-	-	35	mV
I_{OS_TX}	LVDS-Tx Output Short Current	V_{DD}=3.3V	V_{out}=GND	-28	-	-	mA
I_{OZ_TX}	LVDS-Tx Output Tri-state Current	PD=GND	V_{out}=GND to VDD	-10	-	+10	μA

AC Specifications

Table 11. AC Specifications

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{LT}	Phase Lock Loop Set Time (Fig.5)	-	-	-	-	1	ms
t_{DL}	Data Latency (Fig.6)	Dual-In/Dual-Out	CLKIN=85MHz	$9t_{RCP}+3$	$9t_{RCP}+5$	$9t_{RCP}+7$	ns
		Distribution	CLKIN=85MHz	$9t_{RCP}+3$	$9t_{RCP}+5$	$9t_{RCP}+7$	
		Single-In/Dual-Out	CLKIN=85MHz	$(11+2/7)t_{RCP}+3$	$(11+2/7)t_{RCP}+5$	$(11+2/7)t_{RCP}+7$	
		Dual-In/Single-Out	CLKIN=42.5MHz	$(8+5/14)t_{RCP}+3$	$(8+5/14)t_{RCP}+5$	$(8+5/14)t_{RCP}+7$	
t_{DEH}	DE Input High Time (Fig.7)	Single-In/Dual-Out	-	$2t_{RCP}$	-	-	ns
t_{DEL}	DE Input Low Time (Fig.7)		-	$2t_{RCP}$	-	-	
t_{DEINT}	DE Input Period (Fig.7)		-	$4t_{RCP}$	Must be 2n t_{RCP} (n=integer)	-	

AC Timing Diagrams

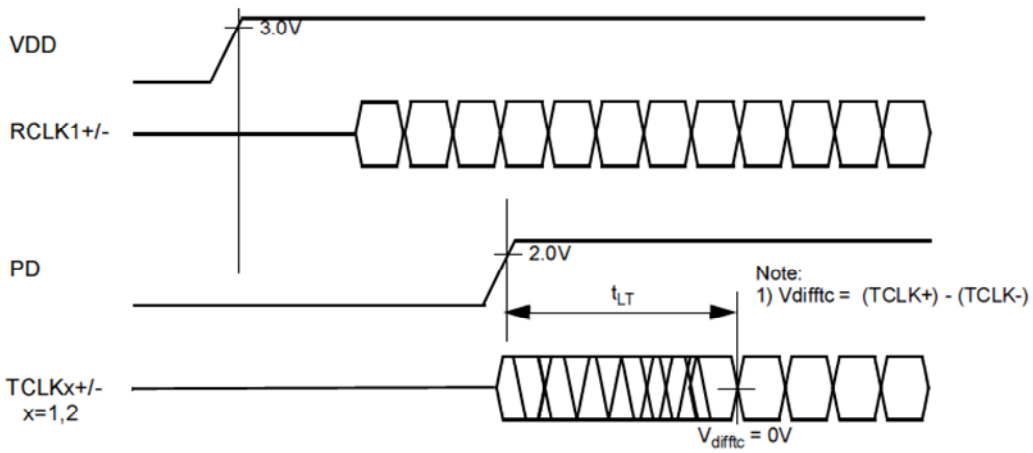


Fig.5 Phase Lock Loop Set Time

AC Timing Diagrams (Continued)

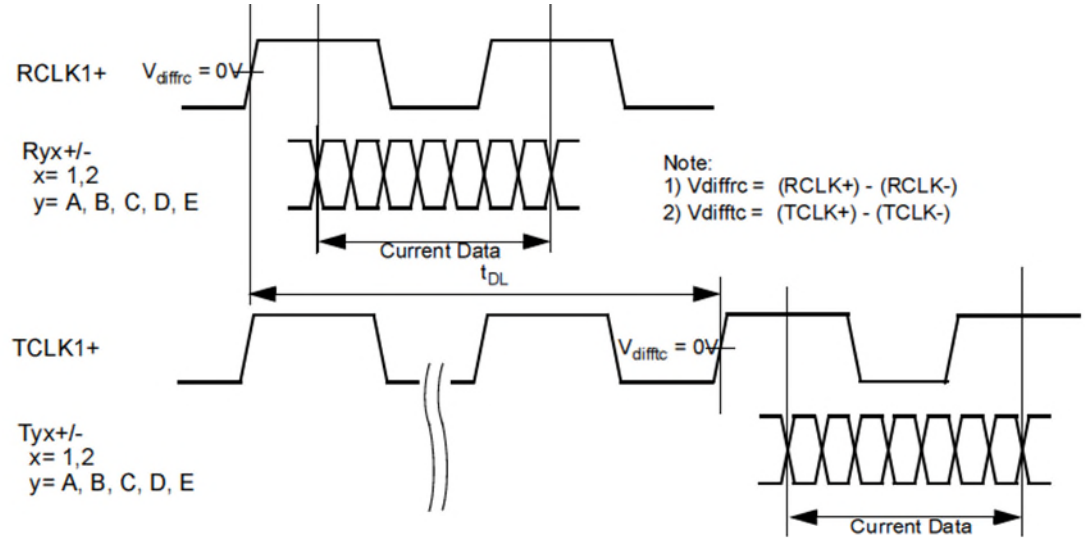


Fig.6 DATA Latency

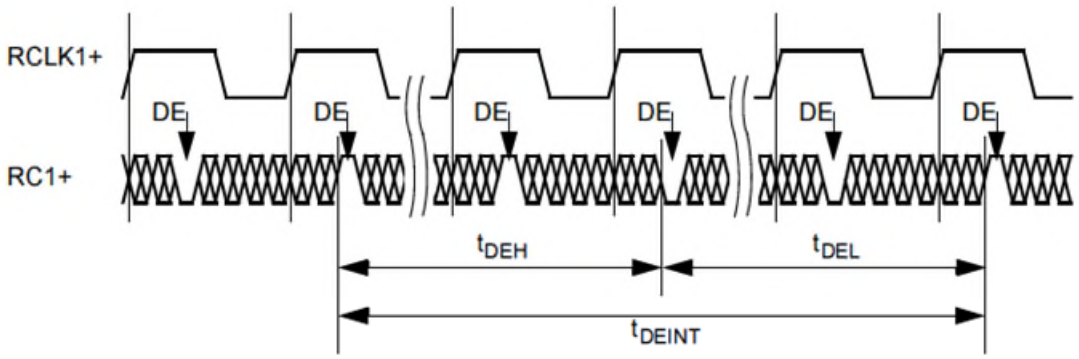


Fig.7 Single Link Input / Dual Link Output Mode RC1(DE) Input Timing

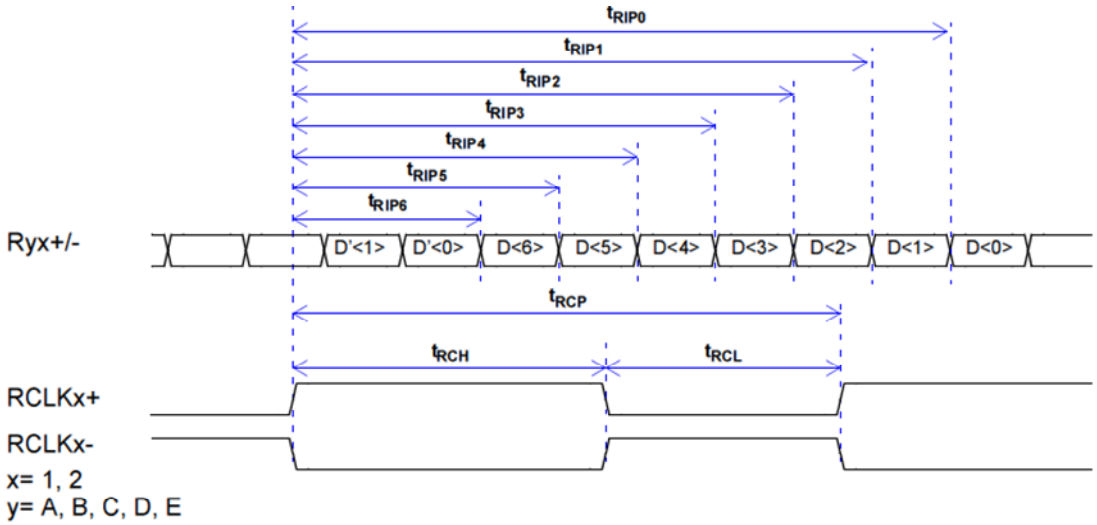
LVDS Receiver AC Specifications

Table 12. LVDS Receiver AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{RCP}	LVDS Clock Period(CLKIN)	-	6.67	-	50	ns
t_{RCH}	LVDS Clock High Duration	-	-	$4/7t_{RCP}$	-	
t_{RCL}	LVDS Clock Low Duration	-	-	$3/7t_{RCP}$	-	
t_{RSUP}	LVDS Data Input Setup Margin	CLKIN=85MHz(1)	480	-	-	ps
		CLKIN=112MHz(1)	250	-	-	
		CLKIN=135MHz(1)	220	-	-	
		CLKIN=150MHz(1)	170	-	-	
t_{RHLD}	LVDS Data Input Hold Margin	CLKIN=85MHz(1)	480	-	-	ps
		CLKIN=112MHz(1)	250	-	-	
		CLKIN=135MHz(1)	220	-	-	
		CLKIN=150MHz(1)	170	-	-	
t_{RIP6}	LVDS Data Input Position 6	-	$2/7t_{RCP}-t_{RHLD}$	$2/7t_{RCP}$	$2/7t_{RCP}+t_{RSUP}$	ps
t_{RIP5}	LVDS Data Input Position 5	-	$3/7t_{RCP}-t_{RHLD}$	$3/7t_{RCP}$	$3/7t_{RCP}+t_{RSUP}$	
t_{RIP4}	LVDS Data Input Position 4	-	$4/7t_{RCP}-t_{RHLD}$	$4/7t_{RCP}$	$4/7t_{RCP}+t_{RSUP}$	
t_{RIP3}	LVDS Data Input Position 3	-	$5/7t_{RCP}-t_{RHLD}$	$5/7t_{RCP}$	$5/7t_{RCP}+t_{RSUP}$	
t_{RIP2}	LVDS Data Input Position 2	-	$6/7t_{RCP}-t_{RHLD}$	$6/7t_{RCP}$	$6/7t_{RCP}+t_{RSUP}$	
t_{RIP1}	LVDS Data Input Position 1	-	$7/7t_{RCP}-t_{RHLD}$	$7/7t_{RCP}$	$7/7t_{RCP}+t_{RSUP}$	
t_{RIP0}	LVDS Data Input Position 0	-	$8/7t_{RCP}-t_{RHLD}$	$8/7t_{RCP}$	$8/7t_{RCP}+t_{RSUP}$	
t_{CK12}	Skew Time Between RCLK1 and RCLK2	-	$-0.3\ t_{RCP}$	-	$+0.3\ t_{RCP}$	ps

(1) V_{IC_RX}=1.2V, t_{RCH}=4/7 t_{RCP}

LVDS Receiver Input Timing



Ry1+/- skew margin is the one between RCLK1+/- and Ry1+/-.

Ry2+/- skew margin is the one between RCLK2+/- and Ry2+/-.

Fig.8 LVDS Receiver Timing

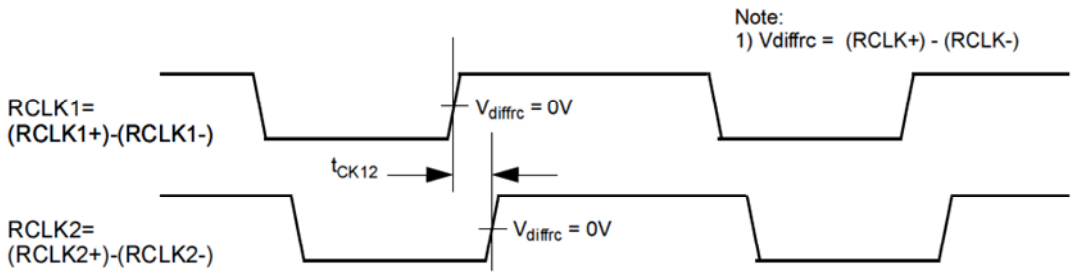


Fig.9 Skew time between RCLK1 and RCLK2

LVDS Transmitter AC Specifications

Table 13. LVDS Transmitter AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{TCP}	LVDS Clock Period(CLKOUT)	-	11.76	-	50	ns
t_{TCH}	LVDS Clock High Duration	-	-	$4/7t_{TCP}$	-	
t_{TCL}	LVDS Clock Low Duration	-	-	$3/7t_{TCP}$	-	
t_{TSUP}	LVDS Data Output Setup	CLKOUT=85MHz	-	-	250	ps
t_{THLD}	LVDS Data Output Hold	CLKOUT=85MHz	-	-	250	ps
t_{TOP6}	LVDS Data Output Position 6	-	$2/7t_{TCP}-t_{THLD}$	$2/7t_{TCP}$	$2/7t_{TCP}+t_{TSUP}$	ps
t_{TOP5}	LVDS Data Output Position 5	-	$3/7t_{TCP}-t_{THLD}$	$3/7t_{TCP}$	$3/7t_{TCP}+t_{TSUP}$	
t_{TOP4}	LVDS Data Output Position 4	-	$4/7t_{TCP}-t_{THLD}$	$4/7t_{TCP}$	$4/7t_{TCP}+t_{TSUP}$	
t_{TOP3}	LVDS Data Output Position 3	-	$5/7t_{TCP}-t_{THLD}$	$5/7t_{TCP}$	$5/7t_{TCP}+t_{TSUP}$	
t_{TOP2}	LVDS Data Output Position 2	-	$6/7t_{TCP}-t_{THLD}$	$6/7t_{TCP}$	$6/7t_{TCP}+t_{TSUP}$	
t_{TOP1}	LVDS Data Output Position 1	-	$7/7t_{TCP}-t_{THLD}$	$7/7t_{TCP}$	$7/7t_{TCP}+t_{TSUP}$	
t_{TOP0}	LVDS Data Output Position 0	-	$8/7t_{TCP}-t_{THLD}$	$8/7t_{TCP}$	$8/7t_{TCP}+t_{TSUP}$	
t_{LVT}	LVDS Transition Time (Fig.11)	-	-	0.6	1.5	ns

LVDS Transmitter Output Diagram

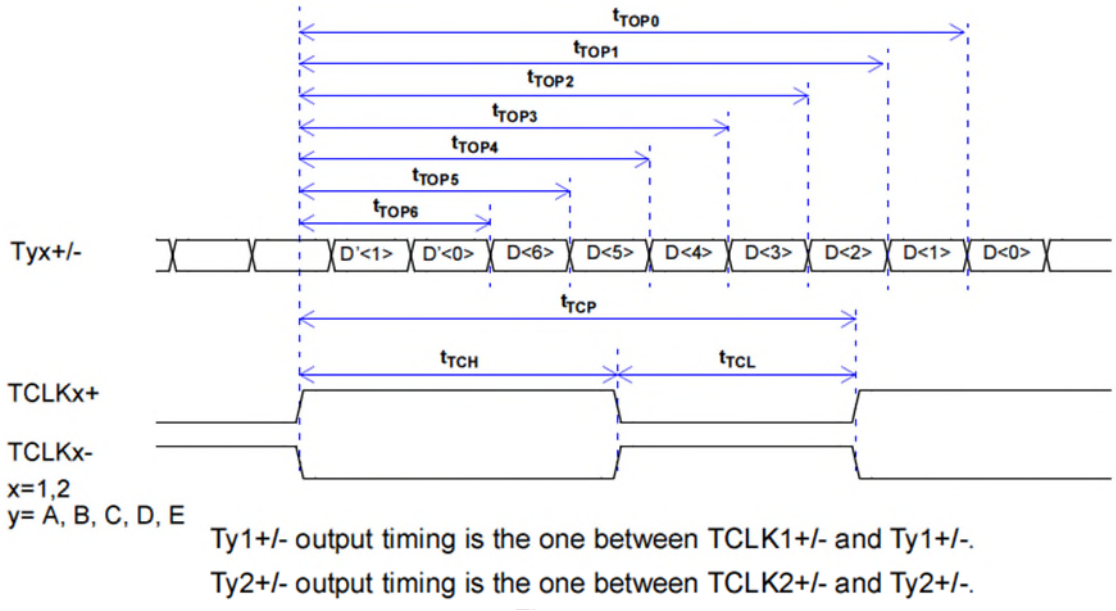


Fig.10 LVDS Transmitter Timing

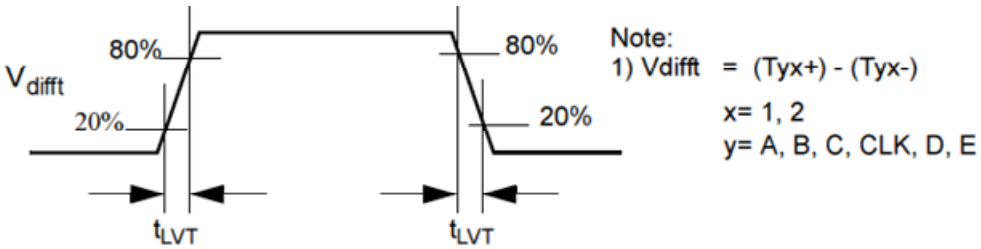
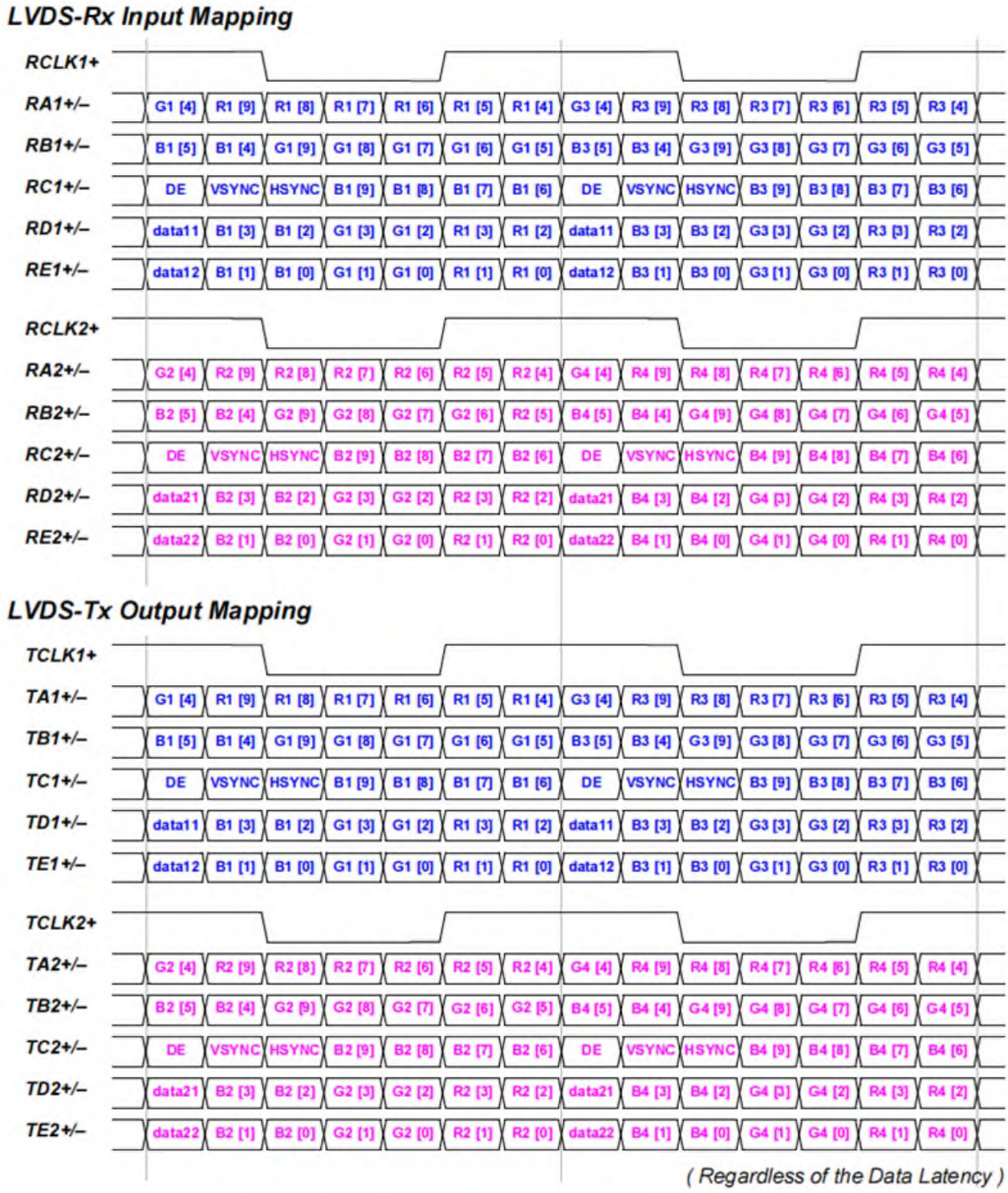


Fig.11 LVDS Transition Timing

LVDS Data Mapping

Dual-In / Dual-Out



Data bits "data11, data12, data21, data22" are available for additional data transmission.

Fig.12-1 Data Mapping for Dual-In/Dual-Out

Distribution Mode

In Distribution mode, RCLK2+/- must be Hi-Z.

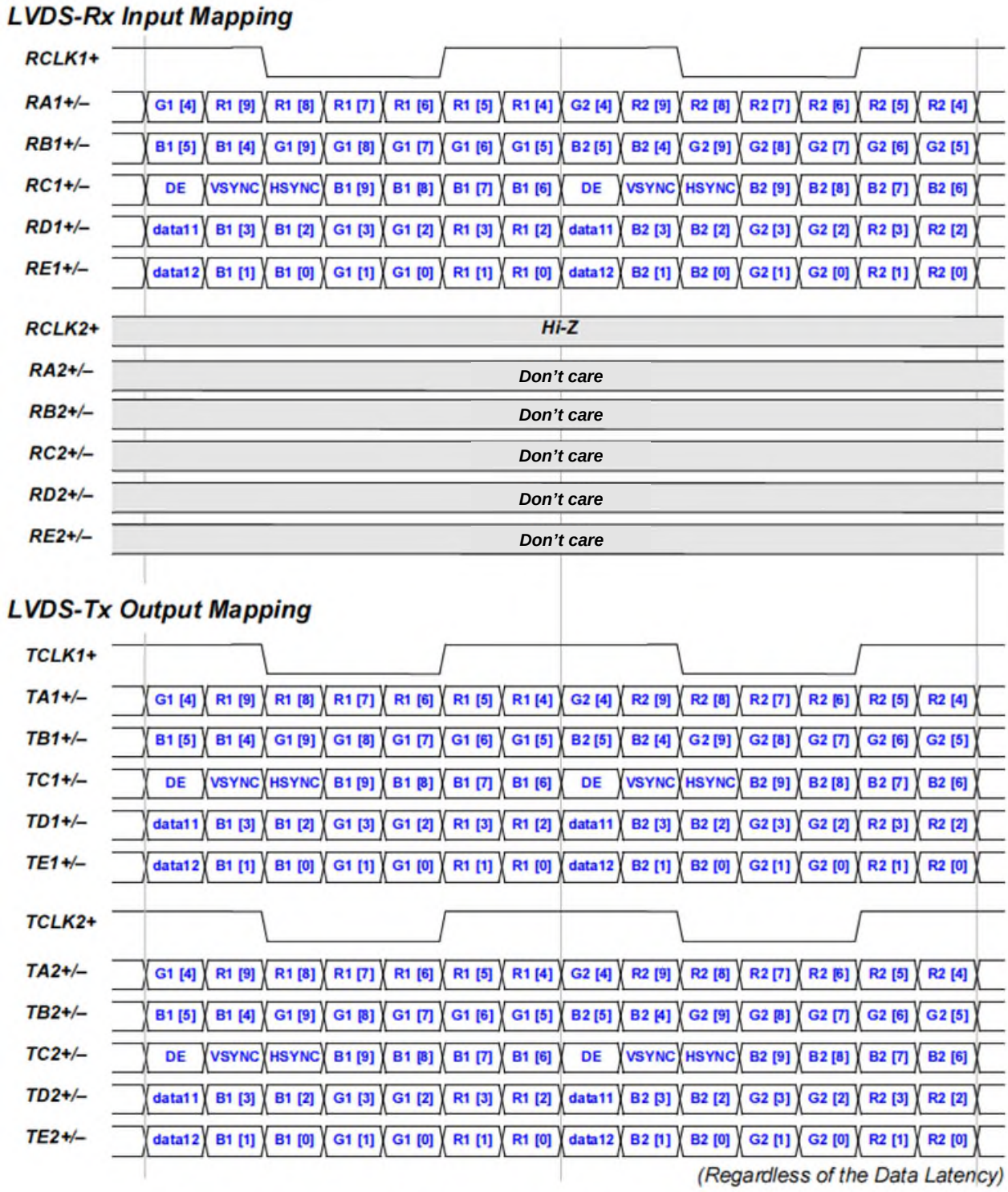
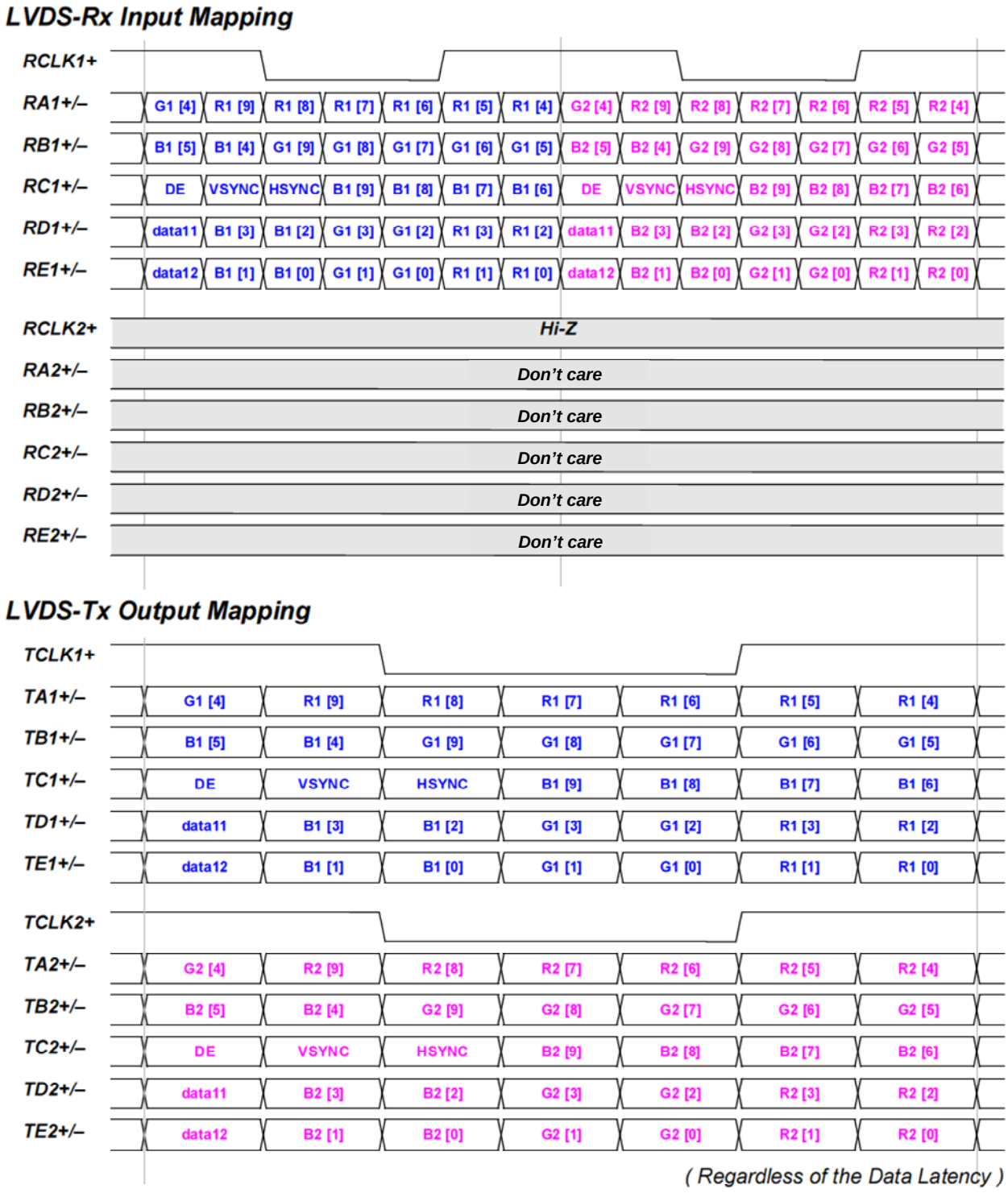


Fig.12-2 Data Mapping for Distribution mode

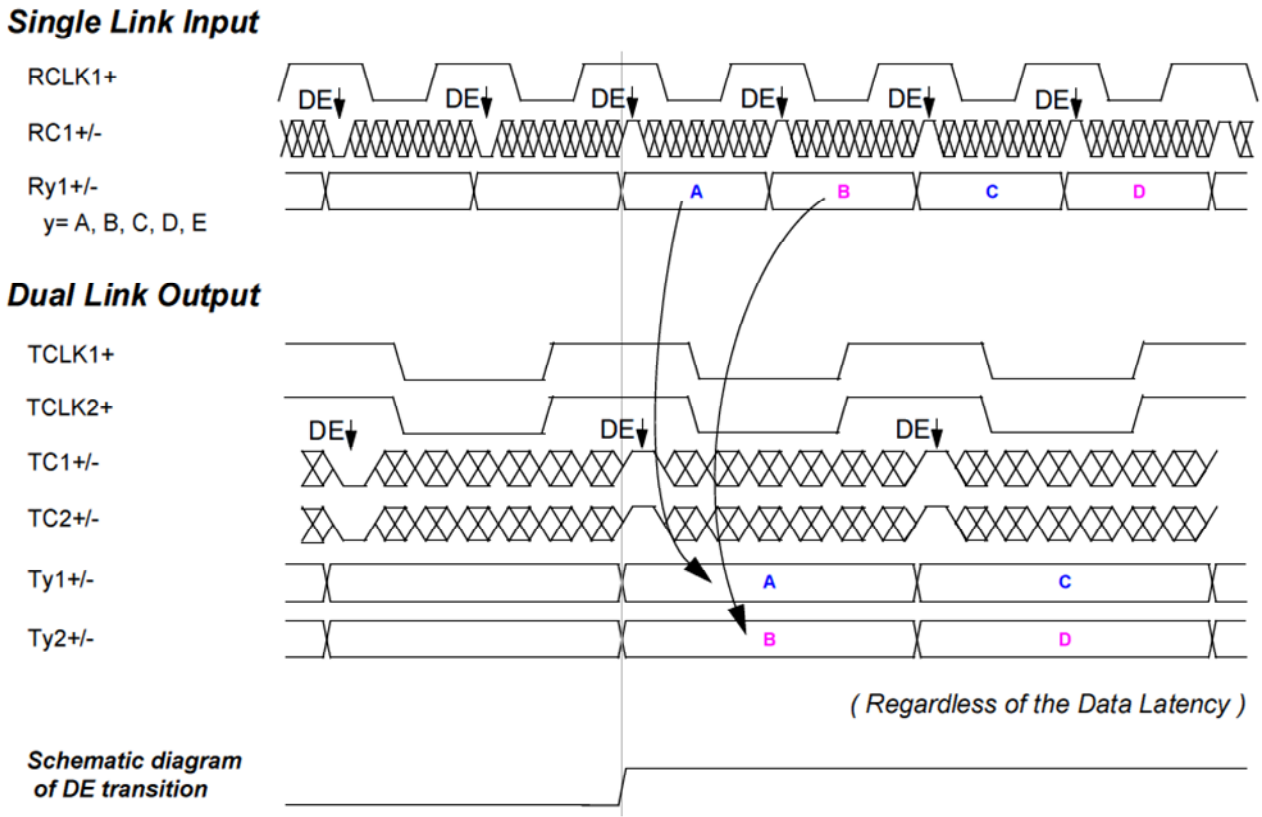
Single-In / Dual-Out

In Single-in / Dual-out mode, RCLK2+/- must be Hi-Z.



Data bits "data11, data12" are available for additional data transmission.

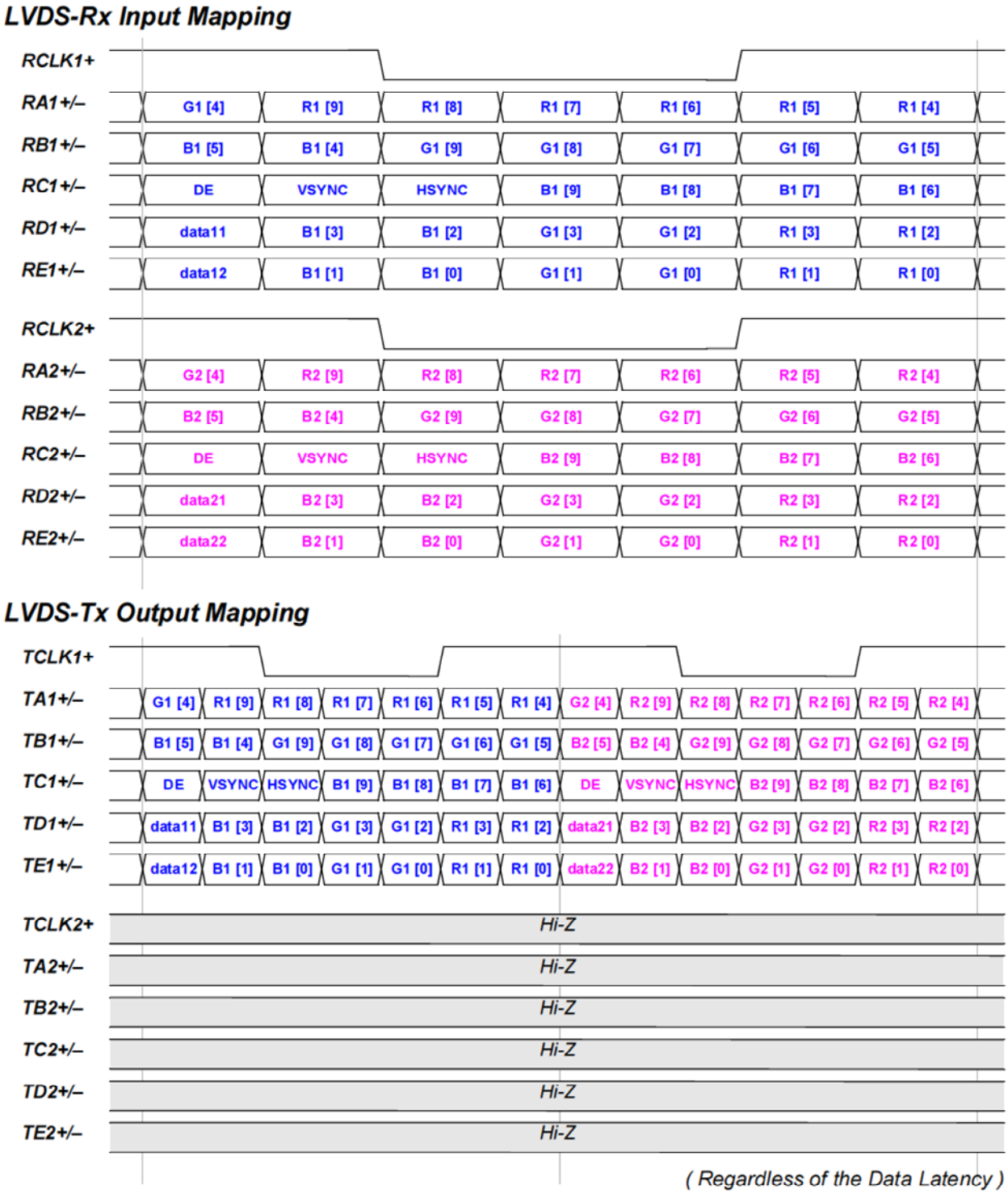
Fig.12-3(a) Data Mapping for Single-In/Dual-Out



Single-in / Dual-out mode uses DE signal L-to-H-edge to start distribution of input data.

Fig.12-3(b) Data Mapping for Single-In/Dual-Out

Dual-In / Single-Out



Data bits "data11, data12, data21, data22" are available for additional data transmission.

Fig.12-4 Data Mapping for Dual-In/Single-Out

Notes

1) LVDS input pin connection

When LVDS line is not derived from the previous device, the line is pulled up to 3.3V internally in THC63LVD1027D. This can cause violation of absolute maximum ratings to the previous LVDS Tx device whose operating condition is lower voltage power supply than 3.3V. This phenomenon may happen at power on phase of the whole system including THC63LVD1027D. One solution for this problem is PD=L control during no LVDS input period because pull-up resistors are cut off at power down state.

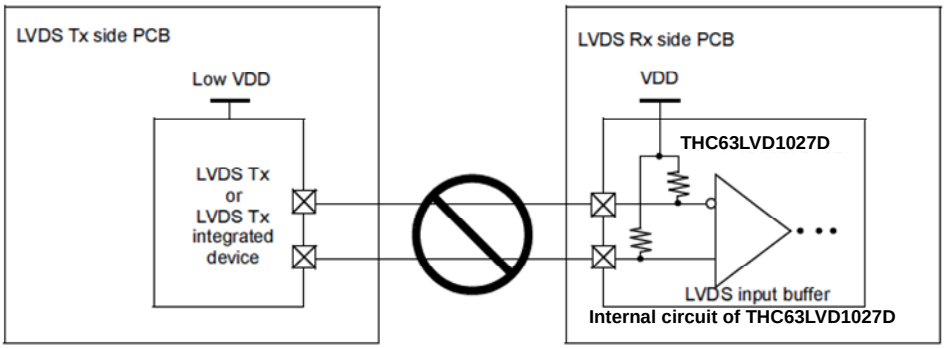


Fig.13 LVDS input pin connection

2) Power On Sequence

Don’t input RCLK1+/- and RCLK2+/- before THC63LVD1027D is on in order to keep absolute maximum ratings.

3) Cable Connection and Disconnection

Don't connect and disconnect the LVDS cable, when the power is supplied to the system.

4) GND Connection

Connect the each GND of the PCB which Transmitter, Receiver and THC63LVD1027D on it.
It is better for EMI reduction to place GND cable as close to LVDS cable as possible.

5) Multi Drop Connection

Multi drop connection is not recommended.

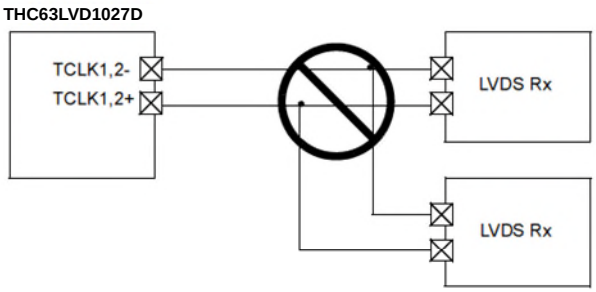


Fig.14 Multi Drop Connection

6) Asynchronous use

Asynchronous use such as following systems are not recommended.
tCK12 spec should be kept.

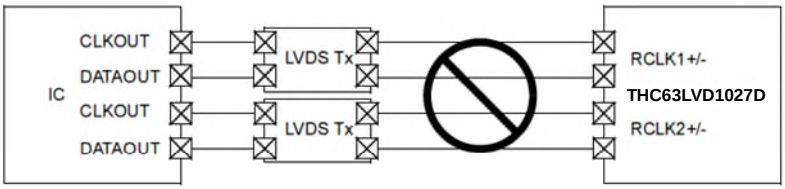


Fig.15-1 Asynchronous Use1

Asynchronous use such as following systems are not recommended.

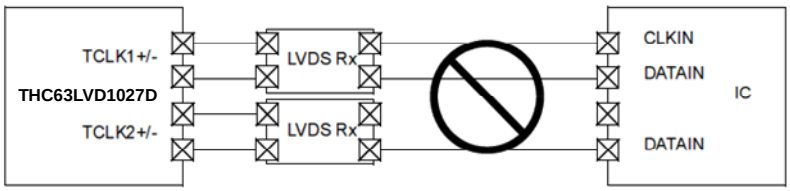


Fig.15-2 Asynchronous Use2

7) De-coupling capacitor

THC63LVD1027D requires appropriate de-coupling capacitor placement on VDD.
Especially, VDD pin 36 and pin 61 requires 0.1uF and 4.7nF capacitor parallel placement close to IC pins.

Package

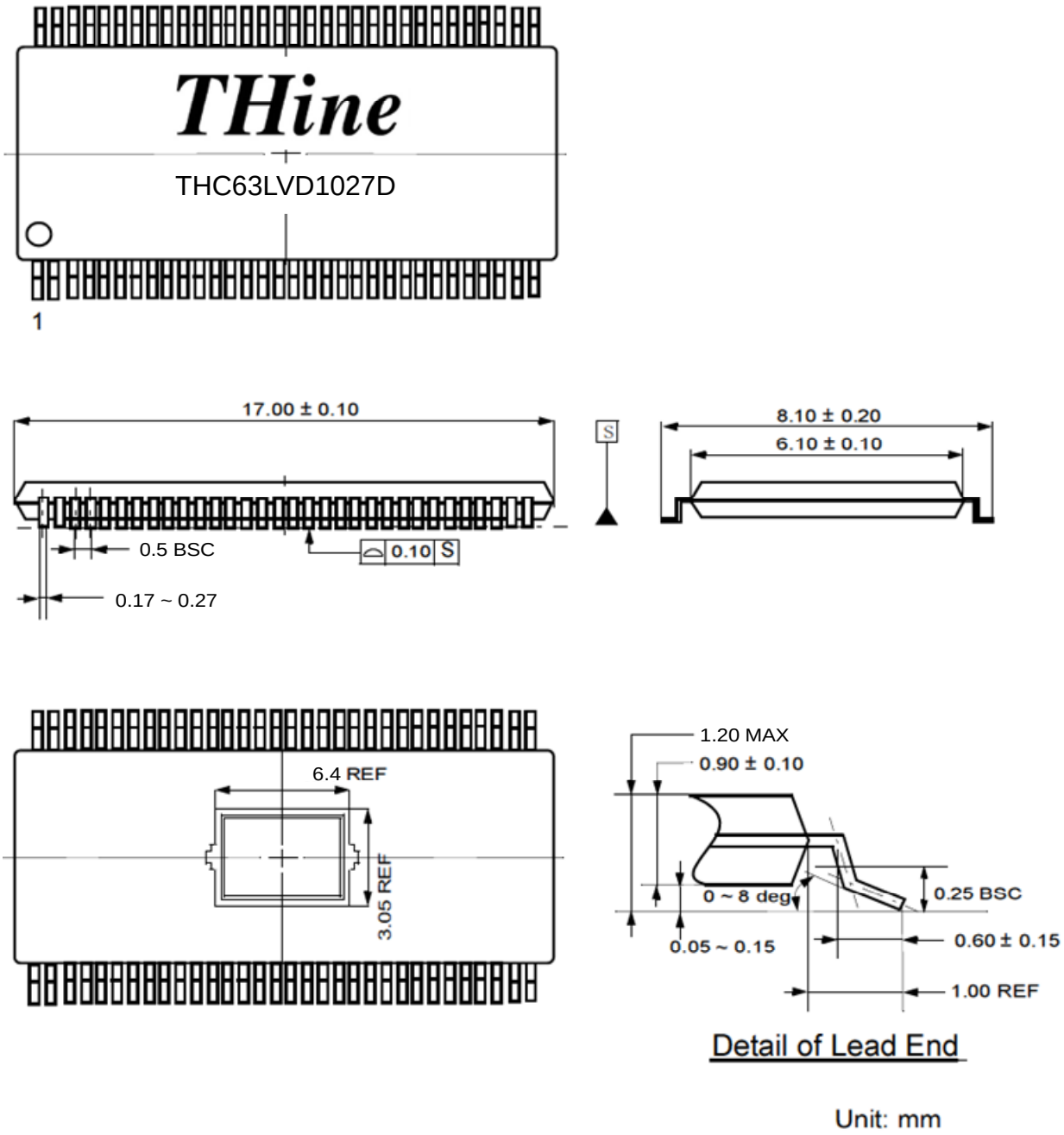


Fig.16 Package Diagram

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