THC63LVDR84B

LVDS 24Bit COLOR HOST-LCD PANEL INTERFACE RECEIVER (Rising Edge Clock)

General Description

The THC63LVDR84B receiver supports wide VCC range(2.5~3.6V). At single 2.5V supply, the THC63LVDR84B reduces EMI and power consumption.
The THC63LVDR84B receiver convert the four LVDS(Low Voltage Differential Signaling) data streams back into 24bits of CMOS/TTL data with rising edge clock.
At a transmit clock frequency of 85MHz, 24bits of RGB data and 4bits of LCD timing and control data (HSYNC, VSYNC, CNTL1, CNTL2) are transmitted at a rate of 2.3Gbps.

Features

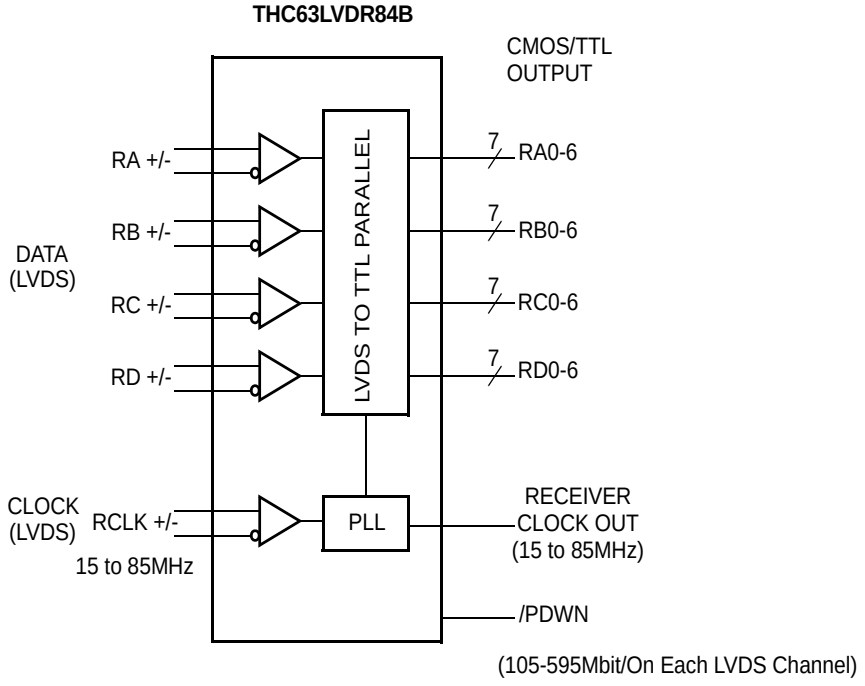
- Wide dot clock and Wide VCC range:

VCC[V]	Clock Frequency[MHz]		
	15 to 20	20 to 70	70 to 85
2.5 to 2.7	n/a	available	n/a
2.7 to 3.0	available	available	n/a
3.0 to 3.6	available	available	available

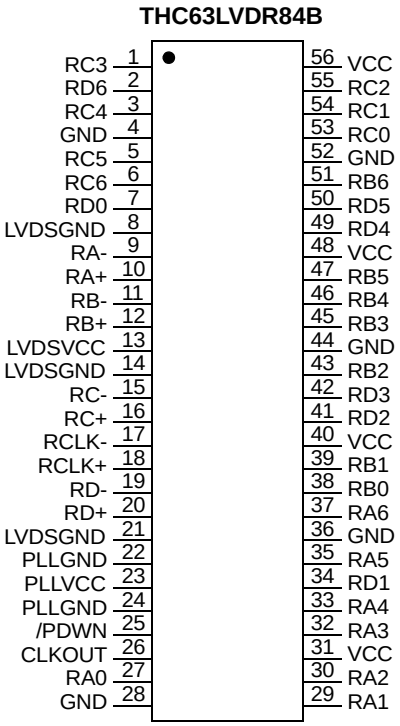
n/a : not available

- Rising Edge Clock
- PLL requires No external components
- Rx power consumption < 80mW @VCC 2.5V, 65MHz Grayscale
- Power-Down Mode
- Low profile 56 Lead TSSOP Package
- Pin compatible with DS90CR286ATMD

Block Diagram



Pin Out



Pin Description

Pin Name	Pin #	Type	Description
RA+, RA-	10, 9	LVDS IN	LVDS Data Inputs
RB+, RB-	12, 11	LVDS IN	
RC+, RC-	16, 15	LVDS IN	
RD+, RD-	20, 19	LVDS IN	
RCLK+, RCLK-	18, 17	LVDS IN	LVDS Clock Inputs
RA0~RA6	27,29,30,32,33,35,37	OUT	Pixel Data Outputs
RB0~RB6	38,39,43,45,46,47,51	OUT	
RC0~RC6	53,54,55,1,3,5,6	OUT	
RD0~RD6	7,34,41,42,49,50,2	OUT	
CLKOUT	26	OUT	Pixel Clock Output
/PDWN	25	IN	H: Normal operation L: Power down (all outputs are pulled to ground)
VCC	31,40,48,56	Power	Power Supply Pins for TTL outputs and digital circuitry
GND	4,28,36,44,52	Ground	Ground Pins for TTL outputs and digital circuitry
LVDSVCC	13	Power	Power Supply Pin for LVDS inputs
LVDSGND	8,14,21	Ground	Ground Pins for LVDS inputs
PLLVCC	23	Power	Power Supply Pin for PLL circuitry
PLLGND	22,24	Ground	Ground Pins for PLL circuitry

Absolute Maximum Ratings

Supply Voltage (V_{CC})	-0.3V ~ +4.0V
CMOS/TTL Input Voltage	-0.3V ~ (V_{CC} + 0.3V)
CMOS/TTL Output Voltage	-0.3V ~ (V_{CC} + 0.3V)
LVDS Receiver Input Voltage	-0.3V ~ (V_{CC} + 0.3V)
Junction Temperature	+125°C
Storage Temperature Range	-55°C ~ +150°C
Reflow Peak Temperature / Time	+260°C / 10sec.
Maximum Power Dissipation @+25°C	1.9W

Recommended Operating Conditions

Parameter		Min.	Max.	Units
All Supply Voltage		2.5	3.6	V
Operating Ambient Temperature		-10	70	°C
Clock Frequency	VCC=2.5V to 2.7V	20	70	MHz
	VCC=2.7V to 3.0V	15	70	MHz
	VCC=3.0V to 3.6V	15	85	MHz

Electrical Characteristics

CMOS/TTL DC SPECIFICATIONS

Vcc = VCC = PVCC = LVCC

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IH}	High Level Input Voltage		2.0		VCC	V
V_{IL}	Low Level Input Voltage		GND		0.8	V
V_{OH1}	High Level Output Voltage	VCC= 3.0V ~ 3.6V I_{OH} = -4mA	2.4			V
V_{OL1}	Low Level Output Voltage	VCC = 3.0V ~ 3.6V I_{OL} = 4mA			0.4	V
V_{OH2}	High Level Output Voltage	VCC= 2.5V ~ 3.0V I_{OH} = -2mA	2.1			V
V_{OL2}	Low Level Output Voltage	VCC = 2.5V ~ 3.0V I_{OL} = 2mA			0.4	V
I_{IN}	Input Current	0V ≤ VIN ≤ VCC			±10	μA

LVDS RECEIVER DC SPECIFICATIONS

Vcc = VCC = PVCC = LVCC

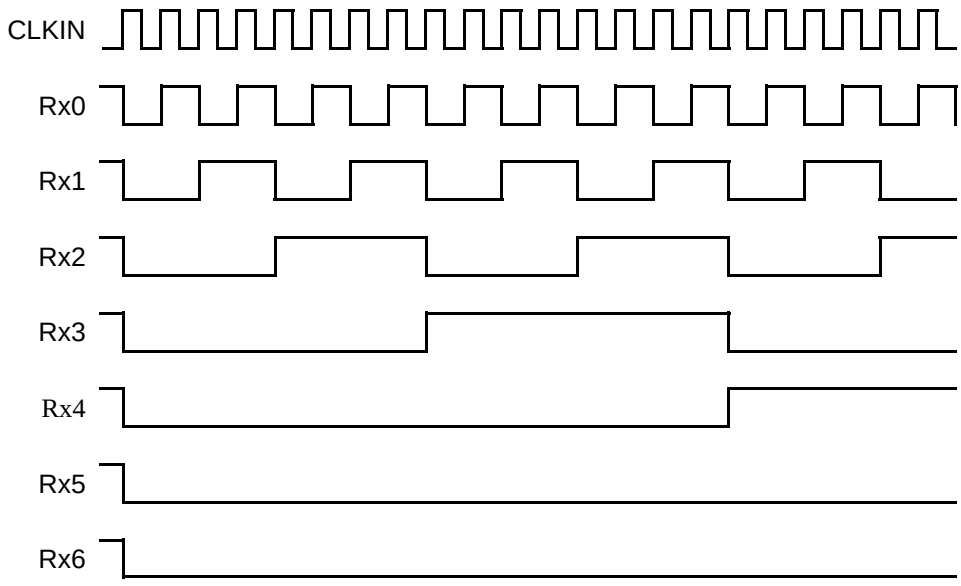
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{TH}	Differential Input High Threshold	VIC = +1.2V			100	mV
V_{TL}	Differential Input Low Threshold		-100			mV
I_{IN}	Input Current	V_{IN} = +2.4V/0V VCC = 3.6V			±10	μA

Supply Current

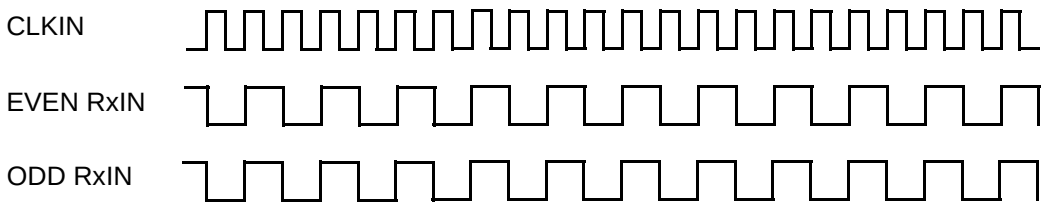
Vcc = VCC = PVCC = LVCC

Symbol	Parameter	Condition(*)		Typ.	Max.	Units
I_{RCCG}	Receiver Supply Current 16Grayscale Pattern	CL=8pF, VCC=3.3V	f = 65MHz	41	53	mA
			f = 85MHz	52	64	mA
		CL=8pF, VCC=2.5V	f = 65MHz	30	42	mA
I_{RCCW}	Receiver Supply Current Worst Case Pattern	CL=8pF, VCC=3.3V	f = 65MHz	72	94	mA
			f = 85MHz	84	96	mA
		CL=8pF, VCC=2.5V	f = 65MHz	42	64	mA
I_{RCCS}	Receiver Power Down Supply Current	/PDWN = L			10	μA

16 Gray Scale Pattern



Worst Case Pattern



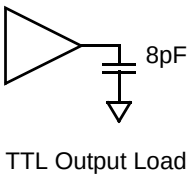
Switching Characteristics

Vcc = VCC = PVCC = LVCC

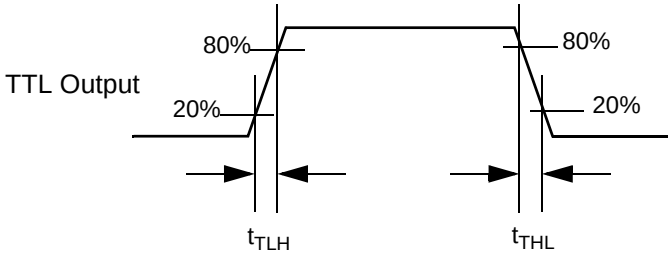
Symbol	Parameter		Min.	Typ.	Max.	Units
t_{RCP}	CLK OUT Period	VCC = 2.5 - 2.7V	14.28	T	50.0	ns
		VCC = 2.7 - 3.0V	14.28	T	66.6	ns
		VCC = 3.0 - 3.6V	11.76	T	66.6	ns
t_{RCH}	CLK OUT High Time			3T/7		ns
t_{RCL}	CLK OUT Low Time			4T/7		ns
t_{RCD}	RCLK +/- to CLK OUT Delay			5T/7		ns
t_{RS}	TTL Data Setup to CLK OUT		0.35T-0.3			ns
t_{RH}	TTL Data Hold from CKL OUT		0.45T-1.6			ns
t_{TLH}	TTL Low to High Transition Time			2.0	3.0	ns
t_{THL}	TTL High to Low Transition Time			1.8	3.0	ns
t_{RIP1}	Input Data Position0 (T = 11.76ns)		-0.4	0.0	0.4	ns
t_{RIP0}	Input Data Position1 (T = 11.76ns)		T/7-0.4	T/7	T/7+0.4	ns
t_{RIP6}	Input Data Position2 (T = 11.76ns)		2T/7-0.4	2T/7	2T/7+0.4	ns
t_{RIP5}	Input Data Position3 (T = 11.76ns)		3T/7-0.4	3T/7	3T/7+0.4	ns
t_{RIP4}	Input Data Position4 (T = 11.76ns)		4T/7-0.4	4T/7	4T/7+0.4	ns
t_{RIP3}	Input Data Position5 (T = 11.76ns)		5T/7-0.4	5T/7	5T/7+0.4	ns
t_{RIP2}	Input Data Position6 (T = 11.76ns)		6T/7-0.4	6T/7	6T/7+0.4	ns
t_{RPLL}	Phase Lock Loop Set				10.0	ms

AC Timing Diagrams

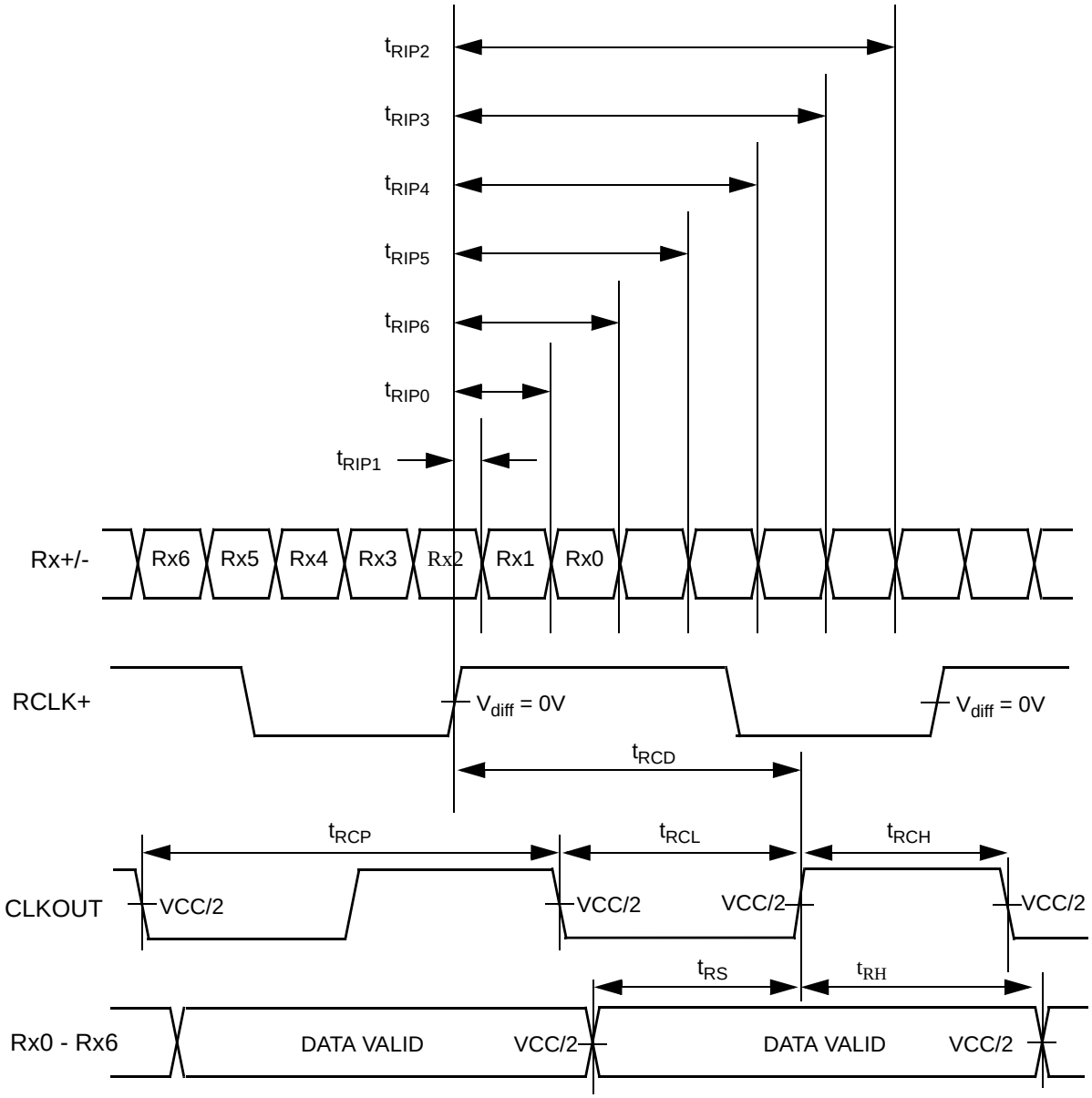
TTL Output



TTL Output Load



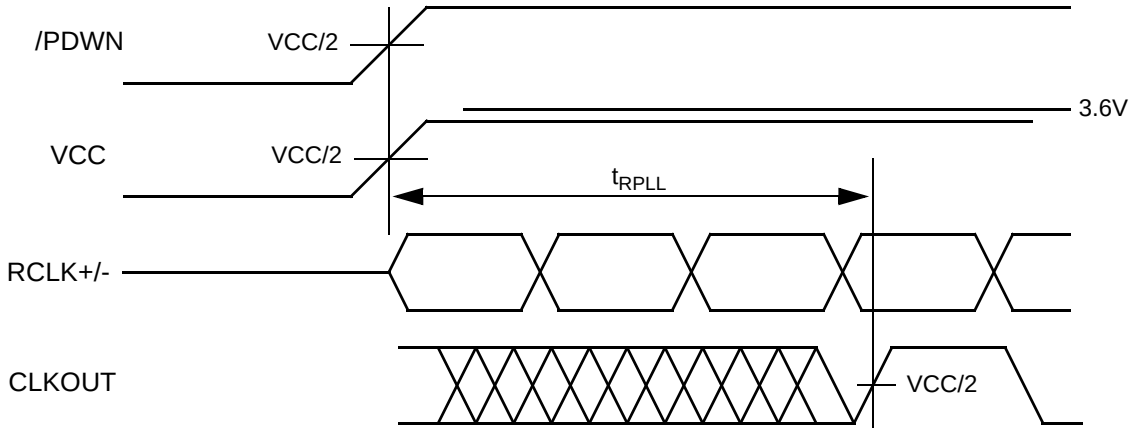
AC Timing Diagrams



Note:
1) Vdiff = (RA+) - (RA-),..... (RCLK+) - (RCLK-)

AC Timing Diagrams

Phase Lock Loop Set Time



Note

1)Power On Sequence

Power on LVDS-Tx after THC63LVDR84B.

2)Cable Connection and Disconnection

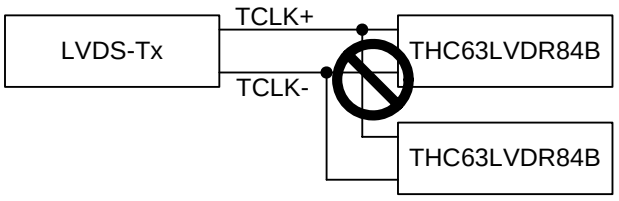
Don't connect and disconnect the LVDS cable, when the power is supplied to the system.

3)GND Connection

Connect the each GND of the PCB which LVDS-Tx and THC63LVDR84B on it. It is better for EMI reduction to place GND cable as close to LVDS cable as possible.

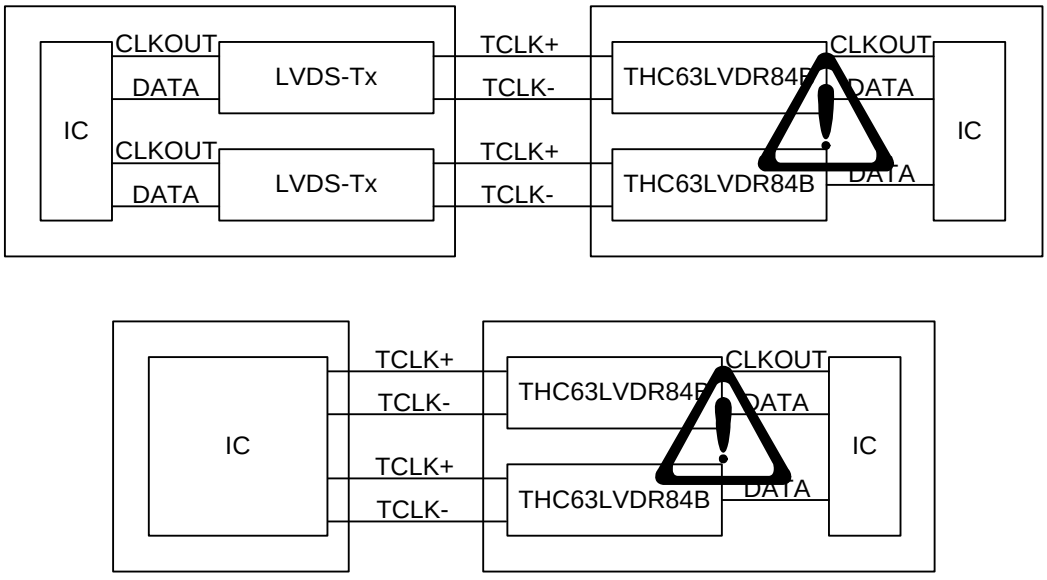
4)Multi Drop Connection

Multi drop connection is not recommended.

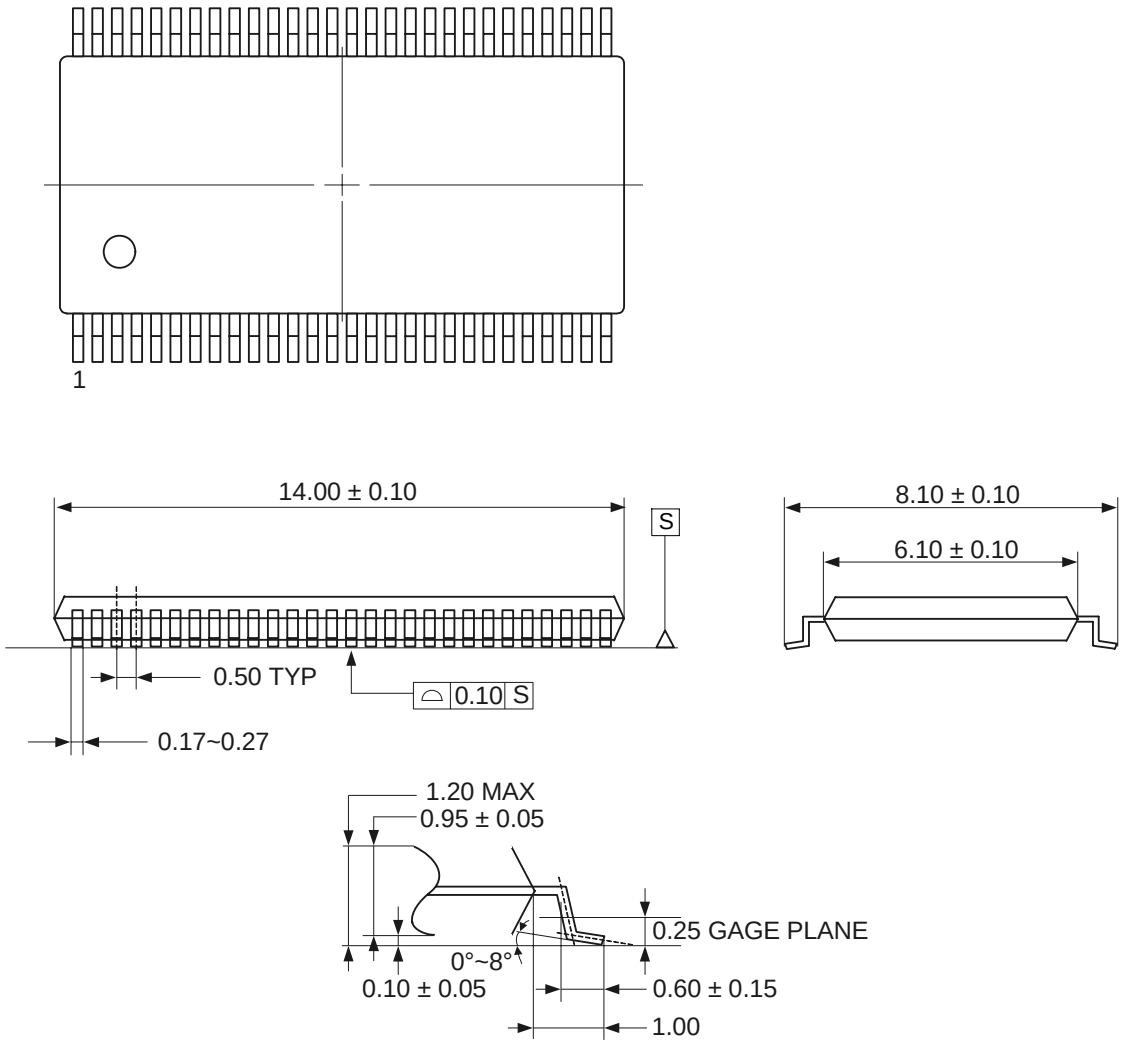


5)Asynchronous use

Asynchronous use such as following systems are not recommended.



Package



Detail of Lead End

Unit:mm

Notices and Requests

1. The product specifications described in this material are subject to change without prior notice.
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