

THCS251

35bit GPIO High Speed Bus Signal Transceiver

System Design Guidelines

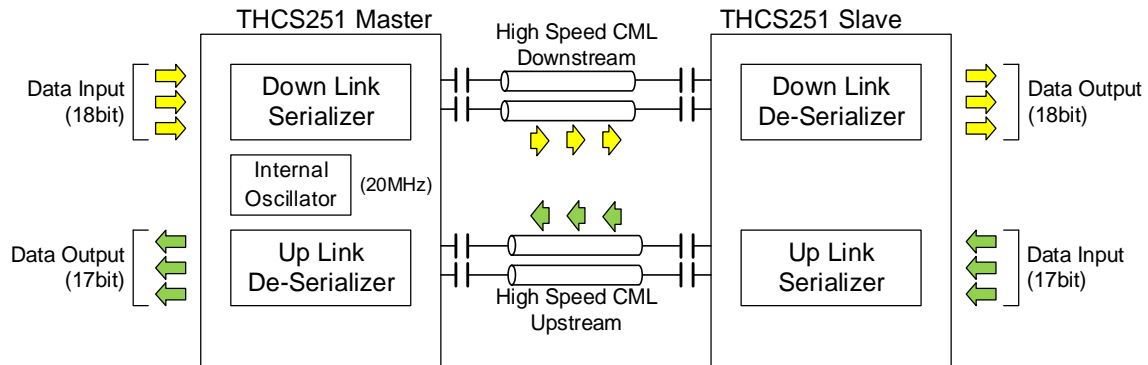
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Connection Selection Guide: Standard Application 1

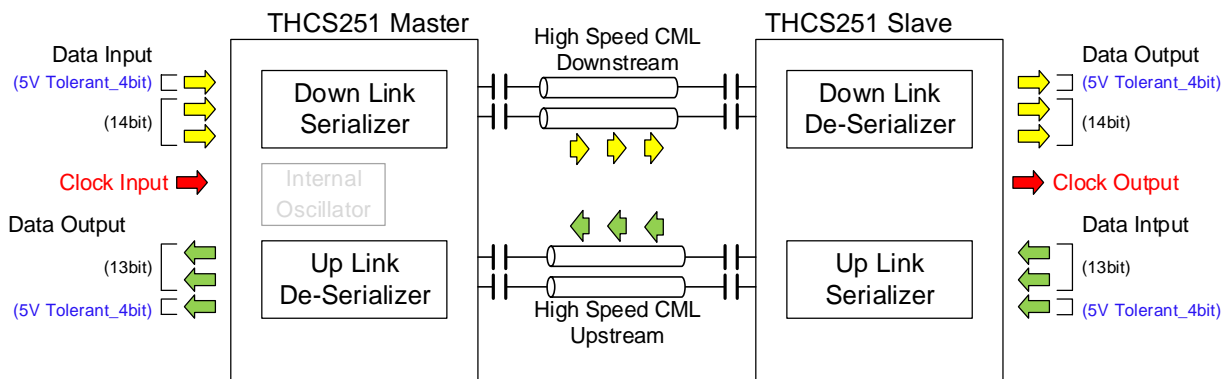
- Example1-1. Bi-directional transmit using internal oscillator. -1-
- Internal clock frequency: 20MHz
- Downstream: 18bit
- Upstream: 17bit
- Output: Push-Pull

[Details: Page.5.]



- Example1-2. Bi-directional transmit using external reference clock. -2-
- Downstream: 18bit
- Upstream: 17bit
- Output: Open-Drain
- *Some I/O Pins are 5V tolerant.

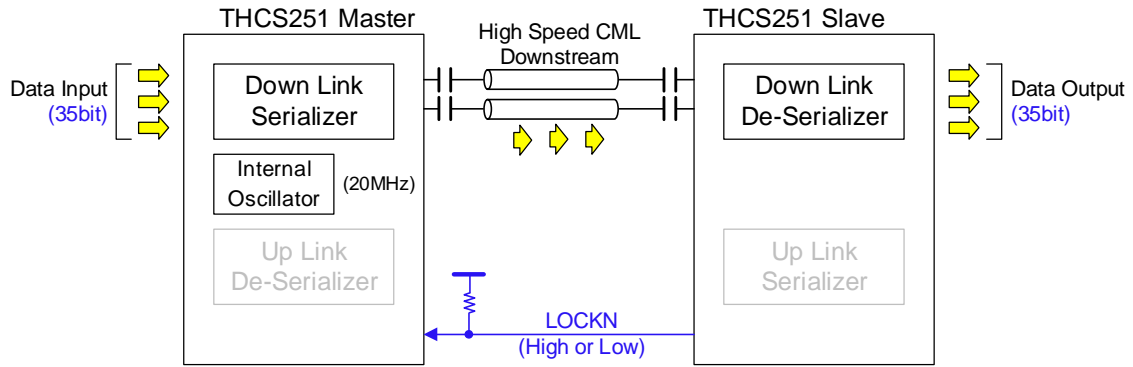
[Details: Page.6]



Connection Selection Guide: Standard Application 2

- Example 2. Uni-directional transmit using internal oscillator
 - Internal clock frequency: 20MHz
 - Downstream: 35bit
 - Upstream: -
 - Output: Push-Pull

[Details: Page.7]



Example1-1. Bi-directional transmit using internal oscillator -1-

This case shows bi-directional transmit 18bit downstream and 17bit upstream using internal oscillator (20MHz). It can be reduced the external parts by using internal oscillator.

Pin settings are as follows.

[Chip-Master/Slave common settings]

- *1. **RESERVED** (#63) is must be tied to Low.
- *2. **DIRSEL0** (#46), **DIRSEL1** (#47) and **DATA_WIDTH** (#50) are set Low to support the 18bit downstream and 17bit upstream.
- *3. **OBUF** (#49) is set High to select Push-Pull output type.

[Only Chip-Master settings]

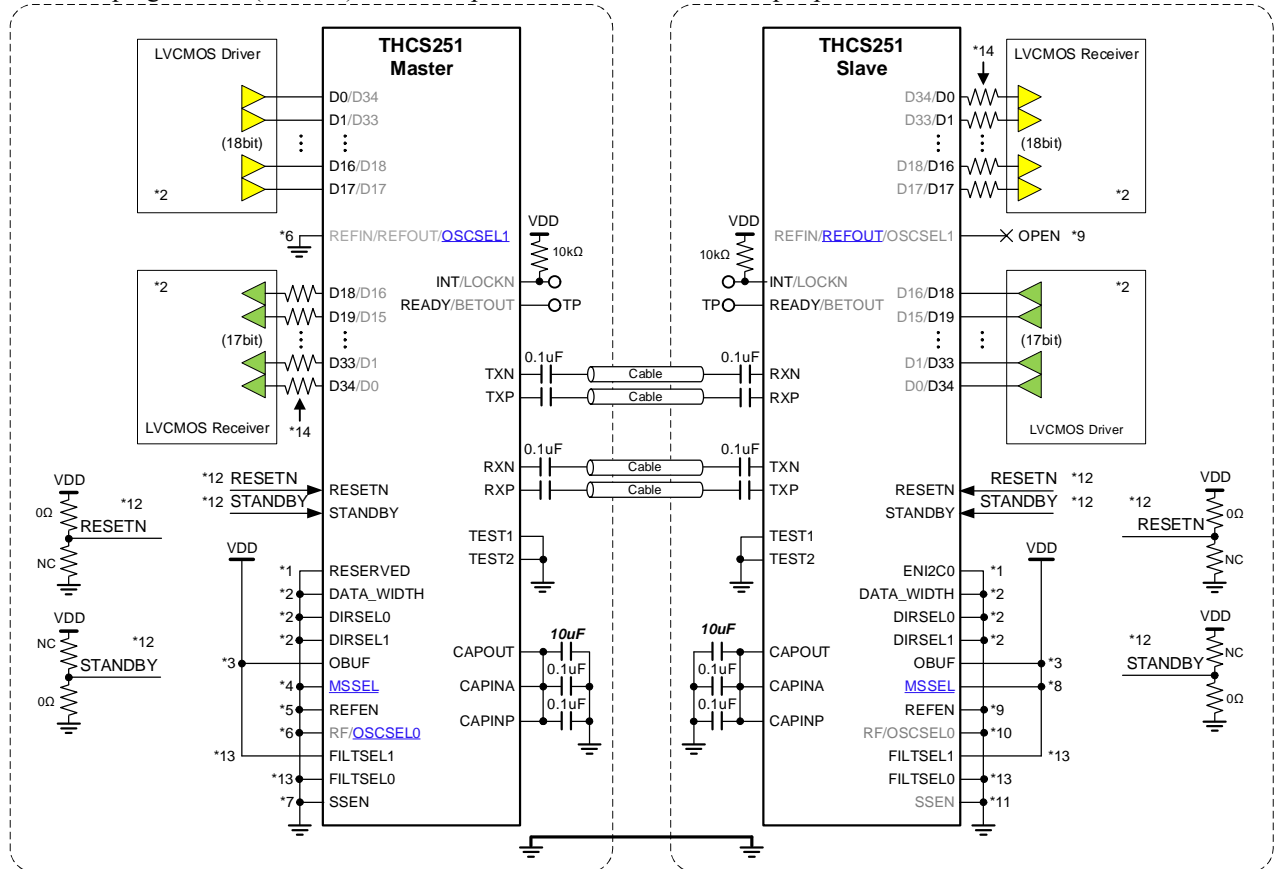
- *4. **MSSEL** (#1) is set Low to select Chip-Master.
- *5. **REFEN** (#45) is set Low to use internal oscillator.
- *6. **RF/OSCSEL0** (#2) and **REFIN/REFOUT/OSCSEL1** (#26) are set Low to select internal oscillator frequency as 20MHz.
- *7. **SSEN** (#4) can be set Spread Spectrum. In this case, the Spread Spectrum is OFF.

[Only Chip-Slave settings]

- *8. **MSSEL** (#1) is set High to select Chip-Slave.
- *9. **REFEN** (#45) is set Low to disable the clock output from **REFIN/REFOUT/OSCSEL1** (#26).
- *10. **RF/OSCSEL0** (#2) is disabled and should be connected to GND.
- *11. **SSEN** (#4) is disabled and should be connected to GND.

[Other settings]

- *12. **RESETN** (#62) and **STANDBY** (#48) can be controlled regardless of the above settings.
- *13. **FILTSEL0** (#5) and **FILTSEL1** (#64) are enabled to control digital filters.
In this case, the digital filter of 8 stages is selected.
- *14. Damping resistor (ex. 33Ω) should be put close each Push-Pull output pin of the device.



Example1-2. Bi-directional transmit using external reference clock -2-

This case shows bi-directional transmit 18bit downstream and 17bit upstream using external reference clock. Pin settings are as follows.

[Chip-Master/Slave common settings]

- *1. **RESERVED** (#63) is must be tied to Low.
- *2. **DIRSEL0** (#46), **DIRSEL1** (#47) and **DATA_WIDTH** (#50) are set Low to support the 18bit downstream and 17bit upstream.
- *3. **OBUF** (#49) is set Low to select Open-Drain output type.

[Only Chip-Master settings]

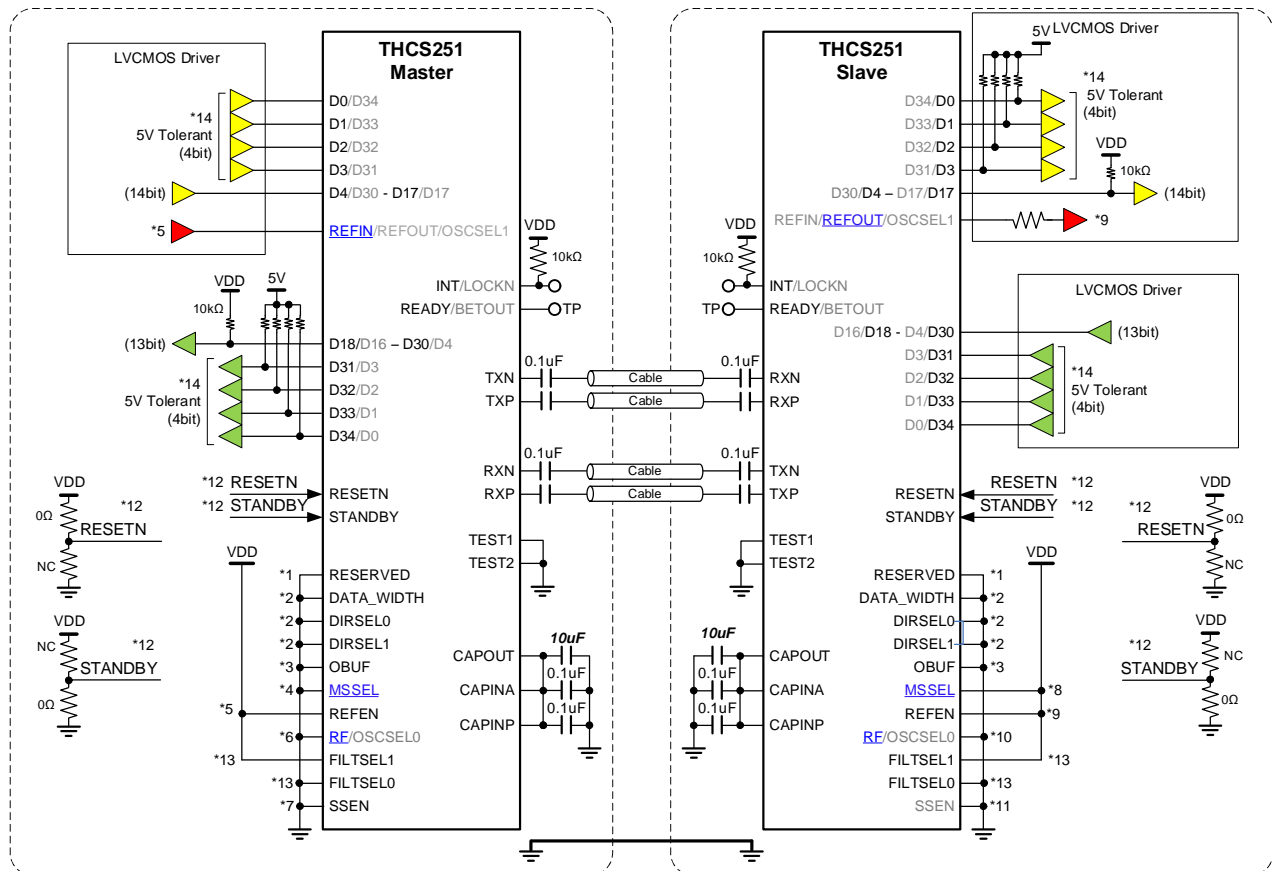
- *4. **MSSEL** (#1) is set Low to select Chip-Master.
- *5. **REFEN** (#45) is set High to use external clock that is input to **REFIN/REFOUT/OSCSEL1** (#26).
- *6. **RF/OSCSEL0** (#2) is enabled and it is adjusted to external clock edge.
- *7. **SSEN** (#4) can be set Spread Spectrum. In this case, the Spread Spectrum is OFF.

[Only Chip-Slave settings]

- *8. **MSSEL** (#1) is set High to select Chip-Slave.
 - *9. **REFEN** (#45) is set High to enable the clock output from **REFIN/REFOUT/OSCSEL1** (#26).
 - *10. **RF/OSCSEL0** (#2) is enabled and adjusted to clock edge of the later device.
- In this case, RF is Low and it is set as Fall Edge.
- *11. **SSEN** (#4) is disabled and should be connected to GND.

[Other settings]

- *12. **RESETN** (#62) and **STANDBY** (#48) can be controlled regardless of the above settings.
 - *13. **FILTSEL0** (#5) and **FILTSEL1** (#64) are enabled to control digital filters.
- In this case, the digital filter of 8 stages is selected.
- *14. Some I/O Pins are 5V tolerant.



Example2. Uni-directional transmit using internal oscillator

This case shows uni-directional transmit 35bit downstream using the internal oscillator (20MHz). It can be reduced the external parts by using internal oscillator. The High Speed Signal line is only 1 Pair. Pin settings are as follows.

[Chip-Master/Slave common settings]

- *1. **RESERVED** (#63) is must to be tied to Low.
- *2. **DIRSEL0** (#46) and **DIRSEL1** (#47) are set High and **DATA_WIDTH** (#50) is set High to support the connection of the 35bit downstream.

[Only Chip-Master settings]

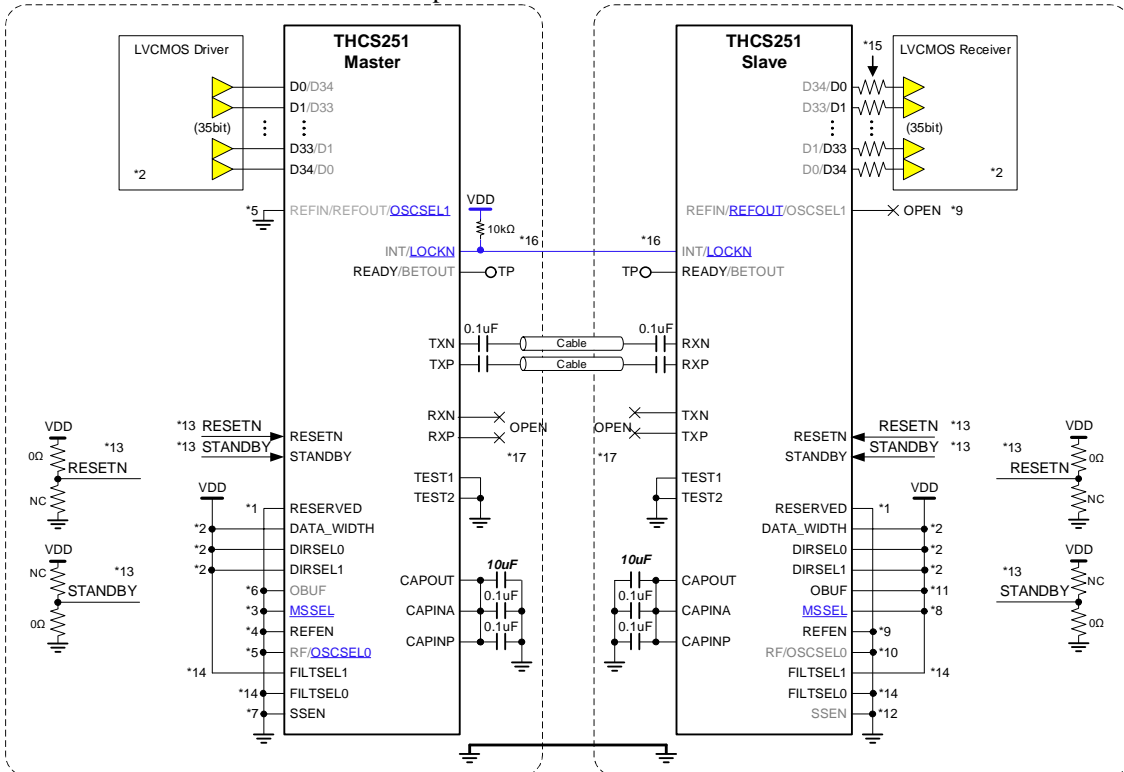
- *3. **MSSEL** (#1) is set Low to select Chip-Master.
- *4. **REFEN** (#45) is set Low to use internal oscillator.
- *5. **RF/OSCSEL0** (#2) and **REFIN/REFOUT/OSCSEL1** (#26) are set Low to select internal oscillator frequency as 20MHz.
- *6. **OBUF** (#49) is disabled and should be connected to GND.
- *7. **SSEN** (#4) can be set the Spread Spectrum. In this case, the Spread Spectrum is OFF.

[Only Chip-Slave settings]

- *8. **MSSEL** (#1) is set High to select Chip-Slave.
- *9. **REFEN** (#45) is set Low to disable the clock output from REFIN/REFOUT/OSCSEL1 (#26).
- *10. **RF/OSCSEL0** (#2) is disabled and should be connected to GND.
- *11. **OBUF** (#49) is set High to select Push-Pull output type.
- *12. **SSEN** (#4) is disabled and should be connected to GND.

[Other settings]

- *13. **RESETN** (#62) and **STANDBY** (#48) can be controlled regardless of the above settings.
- *14. **FILTSEL0** (#5) and **FILTSEL1** (#64) are enabled to control the digital filters. In this case, the digital filter of 8 stages is selected.
- *15. Damping resistor (ex. 33Ω) should be put close each Push-Pull output pin of the device.
- *16. **INT/LOCKN** (#60) is connected to Pull Up at the Chip-Master side.
- *17. Unused **TXN/P** and **RXN/P** should be open.



Design Guideline for Power Supply

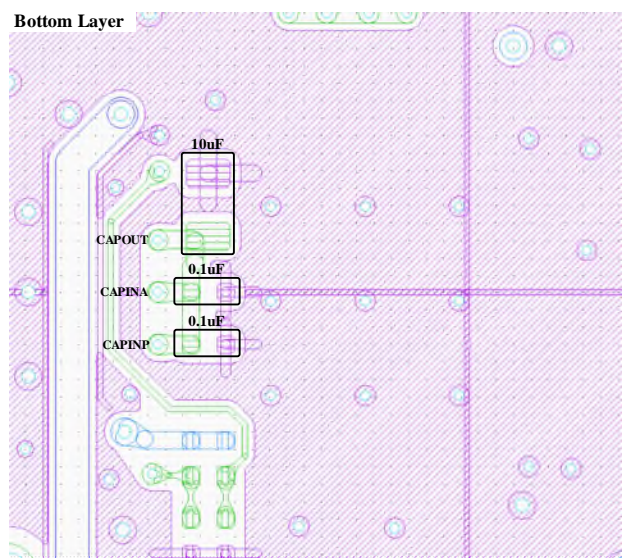
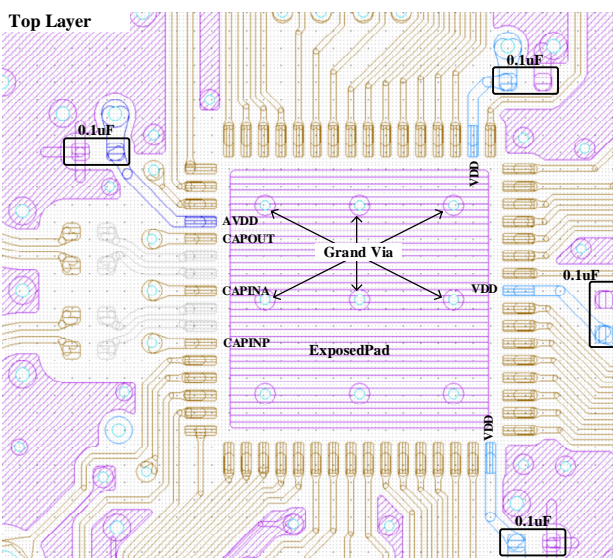
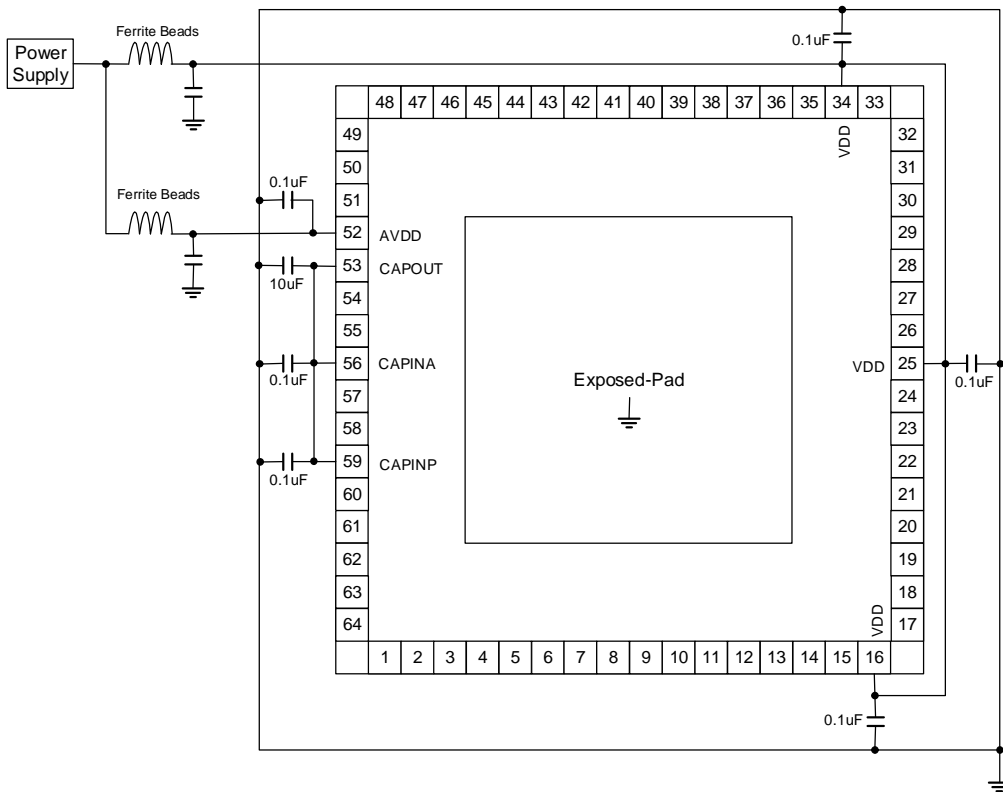
Insert filters (Ferrite Beads and Capacitors) in the Power Supply (**VDD** and **AVDD**).
 And insert Bypass Capacitor (0.1uF) in the Power Supply pins.

This device is equipped with a 1.2V built-in regulator

Insert Bypass Capacitors (**CAPOUT**: 10uF and **CAPINA/CAPINP**: 0.1uF) also for this regulator.

Bypass Capacitors should be attached just near the device.

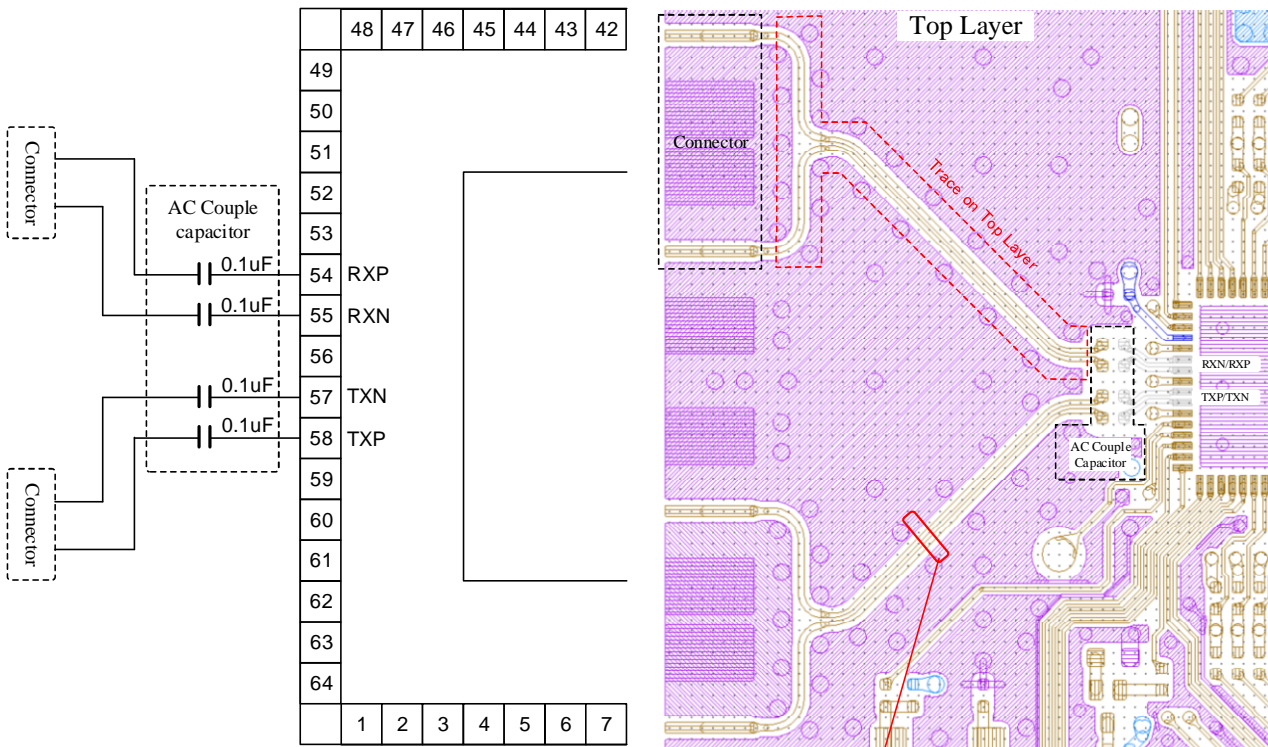
Insert the GND-Via to the Exposed-Pad to strengthen.



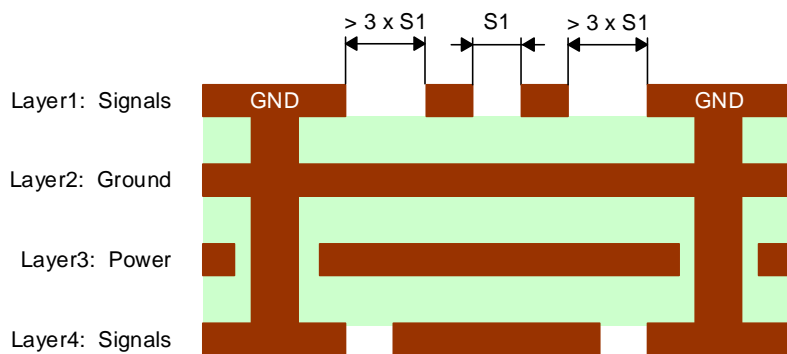
Design Guideline for High-Speed Signal

TXP/TXN and **RXP/RXN** are differential pairs of high-speed serial signals. Differential pairs should be closely spaced and coupled to eliminate common mode noise. Also, differential should be designed as 100Ω differential characteristic impedance (Z_{diff}).

The following is an example of microstrip line design. The high-speed signal lines trace in only single layer. The AC coupled capacitors should be attached just near the device.



Differential signal traces (Microstrip Lines)



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7. Please note that this product is not designed to be radiation-proof.
8. Testing and other quality control techniques are used to this product to the extent THine deems necessary to support warranty for performance of this product. Except where mandated by applicable law or deemed necessary by THine based on the user's request, testing of all functions and performance of the product is not necessarily performed.
9. Customers are asked, if required, to judge by themselves if this product falls under the category of strategic goods under the Foreign Exchange and Foreign Trade Act.
10. The product or peripheral parts may be damaged by a surge in voltage over the absolute maximum ratings or malfunction, if pins of the product are shorted by such as foreign substance. The damages may cause a smoking and ignition. Therefore, you are encouraged to implement safety measures by adding protection devices, such as fuses.