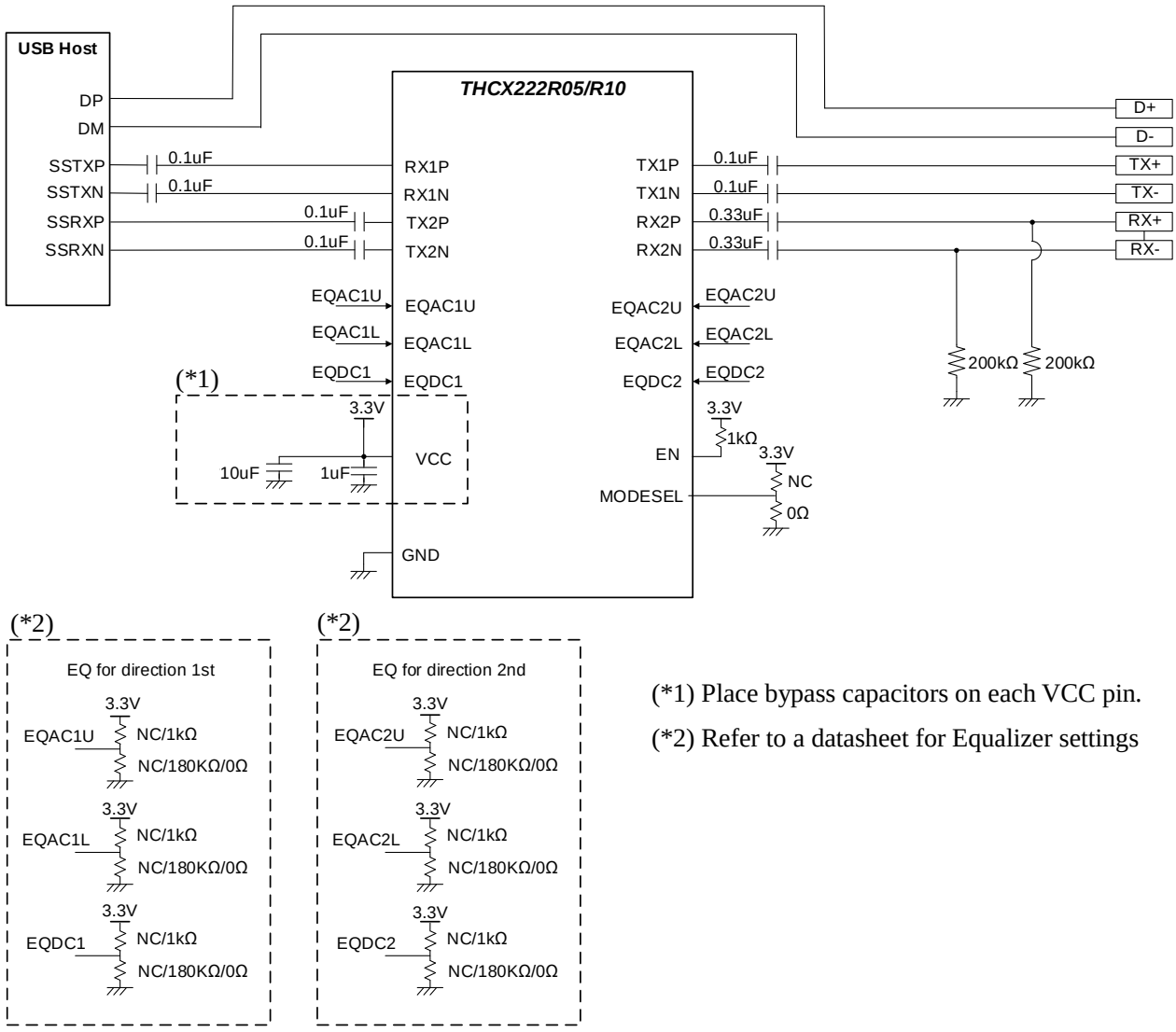
THCX222R05/R10 Design Guide

System Diagram and PCB Design Guideline

Contents

Application diagram

Example:USB3.0/3.1 Gen1 Downstream Facing Port (DFP)



(*1) Place bypass capacitors on each VCC pin.

(*2) Refer to a datasheet for Equalizer settings

Layout guide

- Use at least four-layer PCB with signals, ground, power, and signals assigned for each layer
- PCB traces for high-speed differential signals must be coupled microstrip lines whose differential characteristic impedance is 90Ω±10%.
- Keep differential traces on the layer next to the ground plane, refer to Figure 1.
- Avoid right-angle turns (Figure 2) and minimize the number of vias within 2 or less on the high-speed traces to prevent impedance discontinuity and degrade signal integrity.

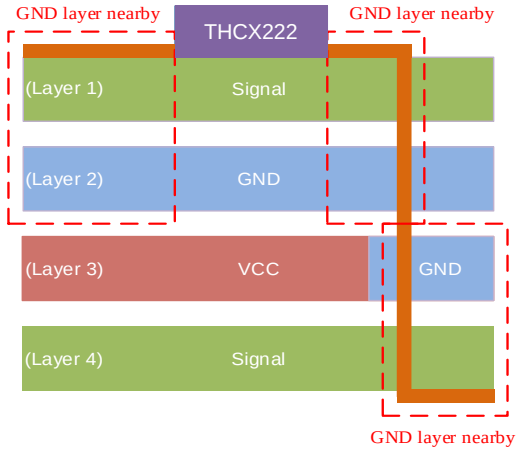


Figure 1. Keep High-speed line next to GND layer

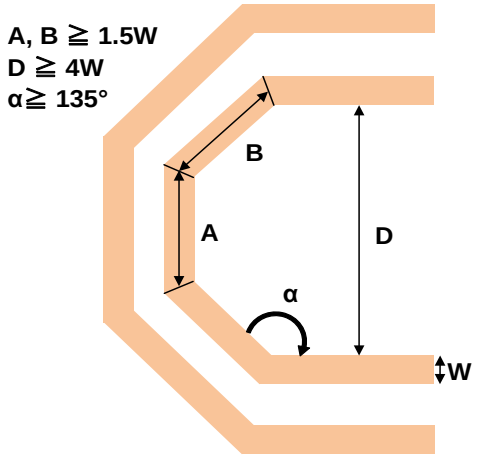
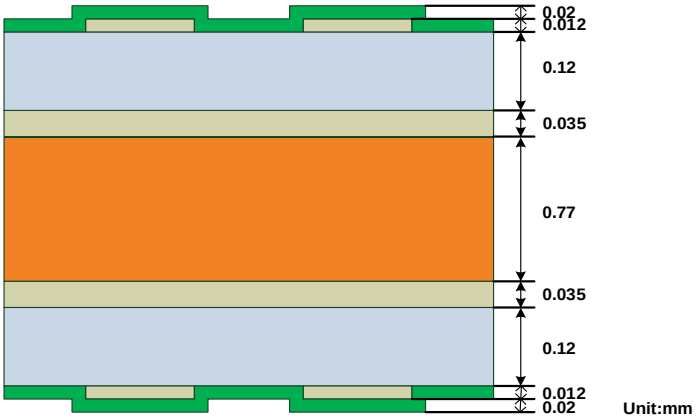


Figure 2. Avoid right angle turn

- Minimize a distance within 5mils between traces of a differential pair to maximize common mode rejection and coupling effect which works to reduce EMI (Electro-Magnetic Interference).
- Distance between a pair should be at least 4 times of the signal trace width.
- Keep away from other high-speed signals.
- Put adjacent GND plane and via between each differential pair for avoiding cross talk.
- Route differential signal traces symmetrically.
- Test points affect signal integrity. You should place test points in series and symmetrically when you need.
- Match the length of differential line at the mismatch location

PCB Stack up example (FR4)



Trace width:	0.17mm
Trace space:	0.13mm
Through hole's diameter:	0.201mm
Through hole's amount:	2

Figure 3. 4 layer PCB stack up example

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