

THC63LVD1023B / THC63LVD1024 Evaluation Kit

LVDS Dual Link Evaluation Board

Parts Number: THEVA1023B, THEVA1024

1. General Description

THEVA1023B and THEVA1024 are designed to evaluate THC63LVD1023B/THC63LVD1024 for transmission video data.

THC63LVD1023B and THC63LVD1024 chipset can transmit 67bit data via dual channel LVDS.

The maximum input clock frequency of THC63LVD1023B is 160MHz, and the maximum output clock frequency of THC63LVD1024 is 135MHz at Dual in / Single out mode.

2. Features

Common Features

- Low power single 3.3V CMOS design
- Power down mode
- Wide dot clock range suited for TV signal(480i to 1080p), PC signal(VGA to QXGA)
- PLL requires no external components
- Clock edge selectable

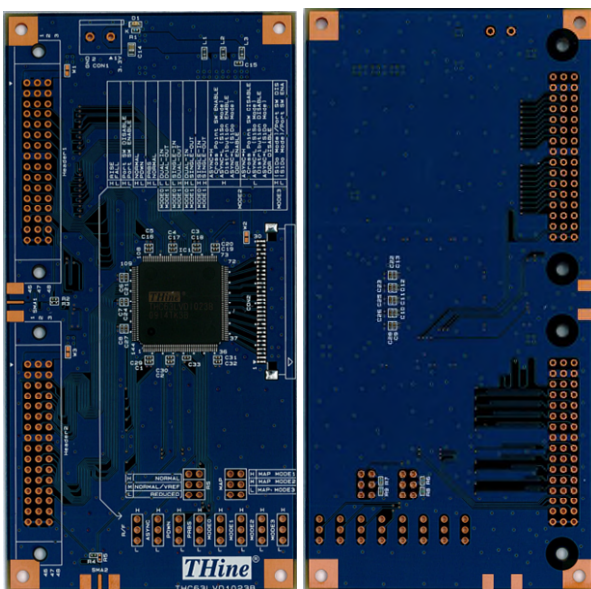
THC63LVD1023B

- Single/Dual TTL in, Single/Dual LVDS out
- Double Edge Input(Single in/Dual out Mode)
- Input Port Switch for Single TTL in/Dual out
- Asynchronous Dual TTL in / Dual LVDS out
- 3 LVDS Data Mapping Modes
- Pseudo Random Pattern Generation Circuit
- Support Reduced Swing LVDS for Lower EMI
- LQFP 144 Pin

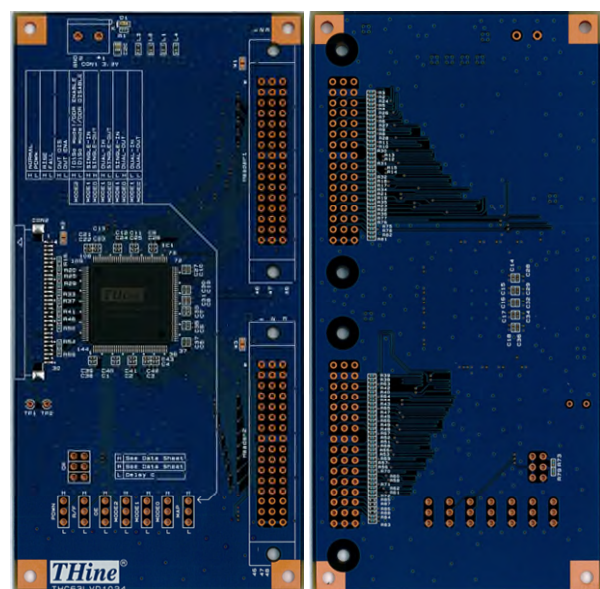
THC63LVD1024

- Single/Dual LVDS in, Single/Dual TTL out
- Double Edge Output
- 50% Output Clock Duty Cycle
- TTL Clock Output Timing Programmable
- 2 Output Data Mapping Modes
- LQFP 144 pin + Exposed Pad

3. Overview



(a)THEVA1023B



(b)THEVA1024

Figure 1 THEVA1023B and THEVA1024

2. Power Supply Setup

This chapter shows power supply condition.

Caution: Please check if there is no power-GND short on below red trace before supplying any power.

3.3V Power Supply to Each Board

Each evaluation board requires 3.3V power supply. Please use “CON1” connector typically.

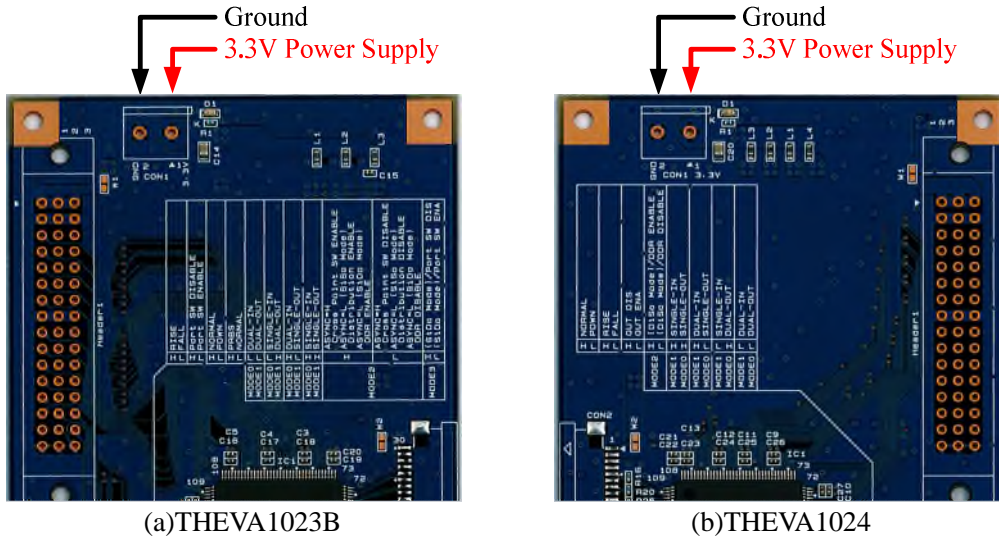


Figure 2 Power Supply for Evaluation Board

Power Supply from / to Connector

3.3V power supply can be connected to Header1 and CON2 by using W1, W2 and W3 solder jumper.

THEVA1023B

- W1: Connect the 3.3V power supply with pin#1, 2 and 3 of Header1.
- W2: Connect the 3.3V power supply with pin#13 and 14 of CON2.
- W3: Connect the 3.3V power supply with pin#1, 2 and 3 of Header2.

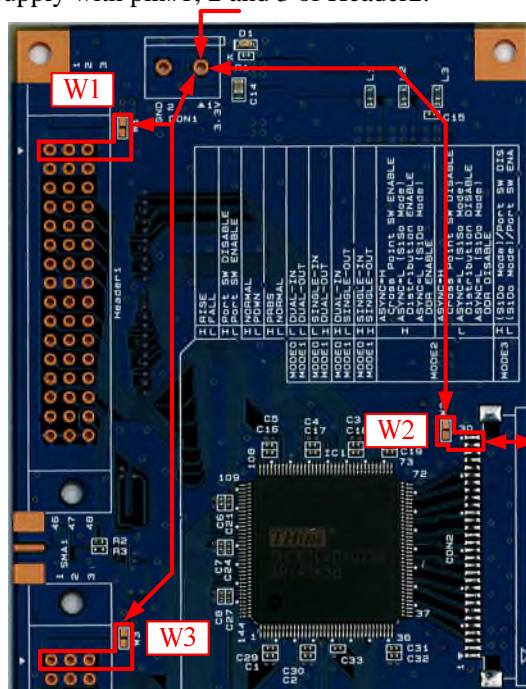


Figure 3 THEVA1023B Power Supply from / to Each Connector

THEVA1024

- W1: Connect the 3.3V power supply with pin#1, 2 and 3 of Header1.
- W2: Connect the 3.3V power supply with pin#1 and 2 of CON2.
- W3: Connect the 3.3V power supply with pin#1, 2 and 3 of Header2.

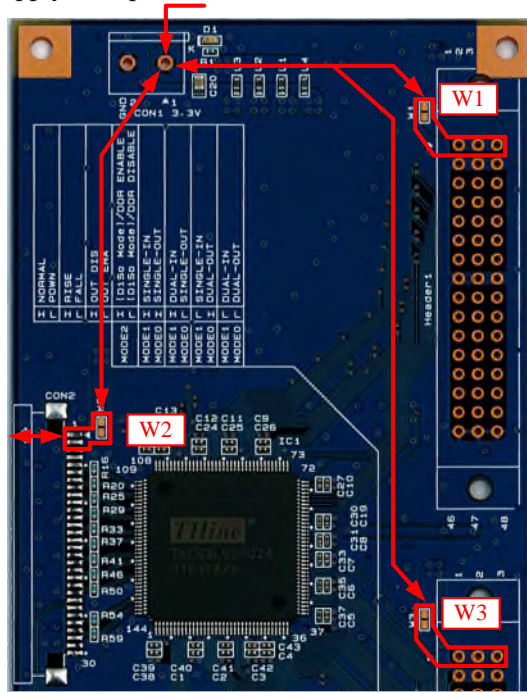
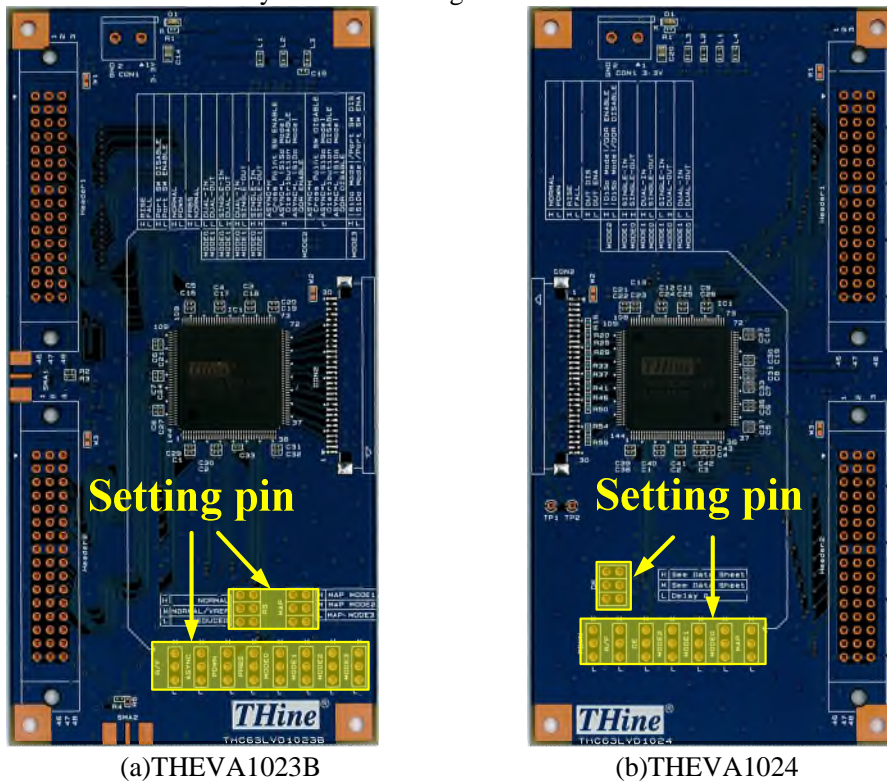


Figure 4 THEVA1024 Power Supply from / to Each Connector

3. Function Setting

Setting pin of each board is shown in yellow area of Figure 5.



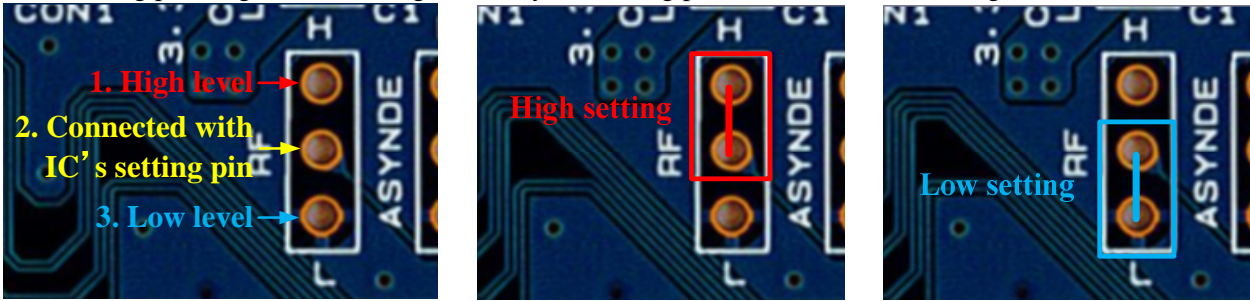
(a)THEVA1023B

(b)THEVA1024

Figure 5 Position of Function Setting Pin

Pin#2 of each 3HEADER is connected to IC's setting pin.

Each setting pin's high or low setting can set by connecting pin#2 of 3HEADER and high level or low level.



(a)3HEADER Description

(b)High Level Setting

(c)Low Level Setting

Figure 6 High / Low Setting Description

THEVA1023B and THEVA1024 have 3 level setting pin.

Please refer to Figure 7 to set the pin into each level.

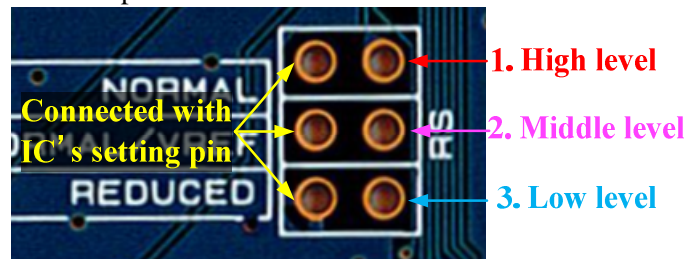
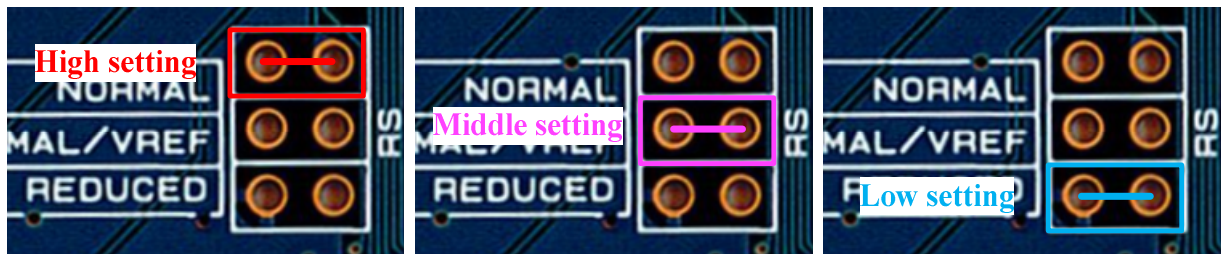


Figure 7 Description of 3Level Setting Pin



(a) High Level Setting

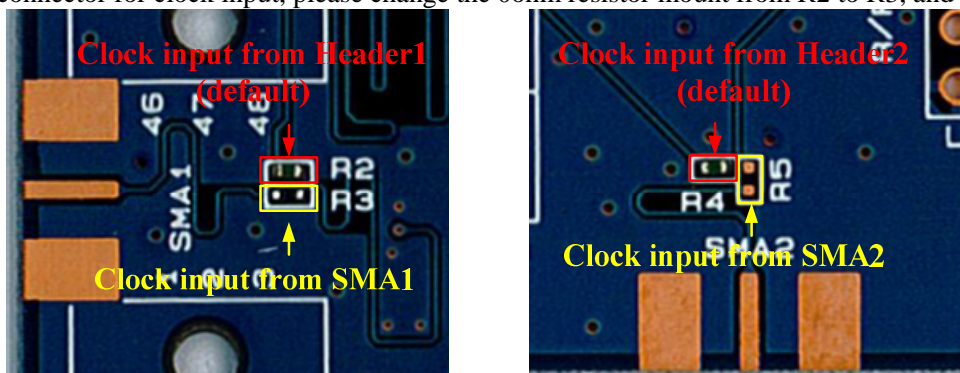
(b) Middle Level Setting

(c) Low Level Setting

Figure 8 High / Middle / Low Setting Description

4. Clock Input from SMA Connector

THEVA1023B can also choose the TTL clock input from SMA connector by using 0ohm resistor. If you want to use SMA connector for clock input, please change the 0ohm resistor mount from R2 to R3, and R4 to R5.



(a)External Clock Input for Channel1

(b)External Clock Input for Channel2

Figure 9 TTL Clock Input Connector Select

5. Status Indicate LED

LED “D1” indicates 3.3V power supply status.

6. Function

This chapter shows function setting of THEVA1023B and THEVA1024.

Table 1 THEVA1023B Function Setting Description

Silk	Symbol	Function																													
RS	RS	LVDS swing mode, VREF select.																													
		<table border="1"> <thead> <tr> <th>RS</th> <th>LVDS Swing</th> <th>Small Swing Input Support</th> </tr> </thead> <tbody> <tr> <td>V_{IHM}</td> <td>350mV</td> <td>N / A</td> </tr> <tr> <td>V_{IMM}</td> <td>350mV</td> <td>RS = V_{REF}</td> </tr> <tr> <td>V_{ILM}</td> <td>200mV</td> <td>N / A</td> </tr> </tbody> </table>	RS	LVDS Swing	Small Swing Input Support	V _{IHM}	350mV	N / A	V _{IMM}	350mV	RS = V _{REF}	V _{ILM}	200mV	N / A																	
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MAP	Mapping Mode																														
V _{IHM}	Mapping MODE1																														
V _{IMM}	Mapping MODE2																														
V _{ILM}	Mapping MODE3																														
MODE3	MODE3	Input port switching function enable when MODE[1:0] = H, L(Single-in / Dual-out). H or Open: Port Switch Disable L: Port Switch Enable																													
MODE2	MODE2	The use of this function depends on the setting of MODE[1:0] or ASYNC.																													
		<table border="1"> <thead> <tr> <th>ASYNC</th> <th>MODE1</th> <th>MODE0</th> <th>Function</th> <th>MODE2</th> <th>Enable / Disable</th> </tr> </thead> <tbody> <tr> <td rowspan="2">H</td> <td rowspan="2">x</td> <td rowspan="2">x</td> <td rowspan="2">Cross Point Switching</td> <td>H</td> <td>Enable</td> </tr> <tr> <td>L</td> <td>Disable</td> </tr> <tr> <td rowspan="4">L</td> <td rowspan="2">H</td> <td rowspan="2">H</td> <td rowspan="2">Distribution Function</td> <td>H</td> <td>Enable</td> </tr> <tr> <td>L</td> <td>Disable</td> </tr> <tr> <td rowspan="2">H</td> <td rowspan="2">L</td> <td rowspan="2">DDR(Double Edge Input) Function</td> <td>H</td> <td>Enable</td> </tr> <tr> <td>L</td> <td>Disable</td> </tr> </tbody> </table>	ASYNC	MODE1	MODE0	Function	MODE2	Enable / Disable	H	x	x	Cross Point Switching	H	Enable	L	Disable	L	H	H	Distribution Function	H	Enable	L	Disable	H	L	DDR(Double Edge Input) Function	H	Enable	L	Disable
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L	L	Dual Link (Dual-in / Dual -out)																													
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H	H	Single Link (Single-in / Single-out)																													
MODE0	MODE0																														
ASYNC	ASYNC	Asynchronous function. H : Asynchronous Function Enable (MODE[1:0] function is enabled in this setting) L : Asynchronous Function Disable (MODE[1:0] function is disabled in this setting)																													
R/F	R/F	Input clock triggering edge select. H : Rising Edge L : Falling Edge																													
PRBS	PRBS	PRBS (Pseudo Random Binary Sequence) generator is active in order to evaluate eye diagram when MODE[1:0] = L, L (Dual-in / Dual-out) or ASYNC = H. H : PRBS Generator Enable L : Normal Operation																													
PDWN	PDWN	Power down function setting H : Normal Operation L : Power Down Mode (All outputs are Hi-Z)																													

Table 2 THEVA1024 Function Setting Description

Silk	Symbol	Function																												
DK	DK	LVDS swing mode, V_{REF} select. <table border="1" style="margin-left: 40px;"> <thead> <tr> <th>MODE1</th> <th>MODE0</th> <th>DK</th> <th>Function</th> </tr> </thead> <tbody> <tr> <td>L L</td> <td></td> <td>L</td> <td>0</td> </tr> <tr> <td>H L</td> <td></td> <td>M</td> <td>$-6(tDOUT)/28$</td> </tr> <tr> <td>H H</td> <td></td> <td>H</td> <td>$6(tDOUT)/28$</td> </tr> <tr> <td>L H</td> <td></td> <td>L</td> <td>0</td> </tr> <tr> <td></td> <td></td> <td>M</td> <td>$-7(tDOUT)/28$</td> </tr> <tr> <td></td> <td></td> <td>H</td> <td>$7(tDOUT)/28$</td> </tr> </tbody> </table>	MODE1	MODE0	DK	Function	L L		L	0	H L		M	$-6(tDOUT)/28$	H H		H	$6(tDOUT)/28$	L H		L	0			M	$-7(tDOUT)/28$			H	$7(tDOUT)/28$
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MODE2	MODE2	DDR function enable. The use of this function depends on the setting MODE[1:0]. <table border="1" style="margin-left: 40px;"> <thead> <tr> <th>MODE1</th> <th>MODE0</th> <th>MODE2</th> <th>Function</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>L</td> <td>Must be tied to GND</td> </tr> <tr> <td>L</td> <td>H</td> <td>H</td> <td>DDR Function Enable</td> </tr> <tr> <td></td> <td></td> <td>L</td> <td>DDR Function Disable</td> </tr> <tr> <td>H</td> <td>L</td> <td>L</td> <td>Must be Tied to GND</td> </tr> <tr> <td>H</td> <td>H</td> <td>L</td> <td>Must be Tied to GND</td> </tr> </tbody> </table>	MODE1	MODE0	MODE2	Function	L	L	L	Must be tied to GND	L	H	H	DDR Function Enable			L	DDR Function Disable	H	L	L	Must be Tied to GND	H	H	L	Must be Tied to GND				
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MODE0	MODE0																													
OE	OE	Output enable H : Output Enable L : Output Disable																												
R/F	R/F	Output clock triggering edge select. H : Rising Edge L : Falling Edge																												
PDWN	PDWN	Power down function setting H : Normal Operation L : Power Down Mode (All outputs are Hi-Z)																												
MAP	MAP	LVDS mapping table select. H : Mapping MODE1 L : Mapping MODE2																												

7. Schematic

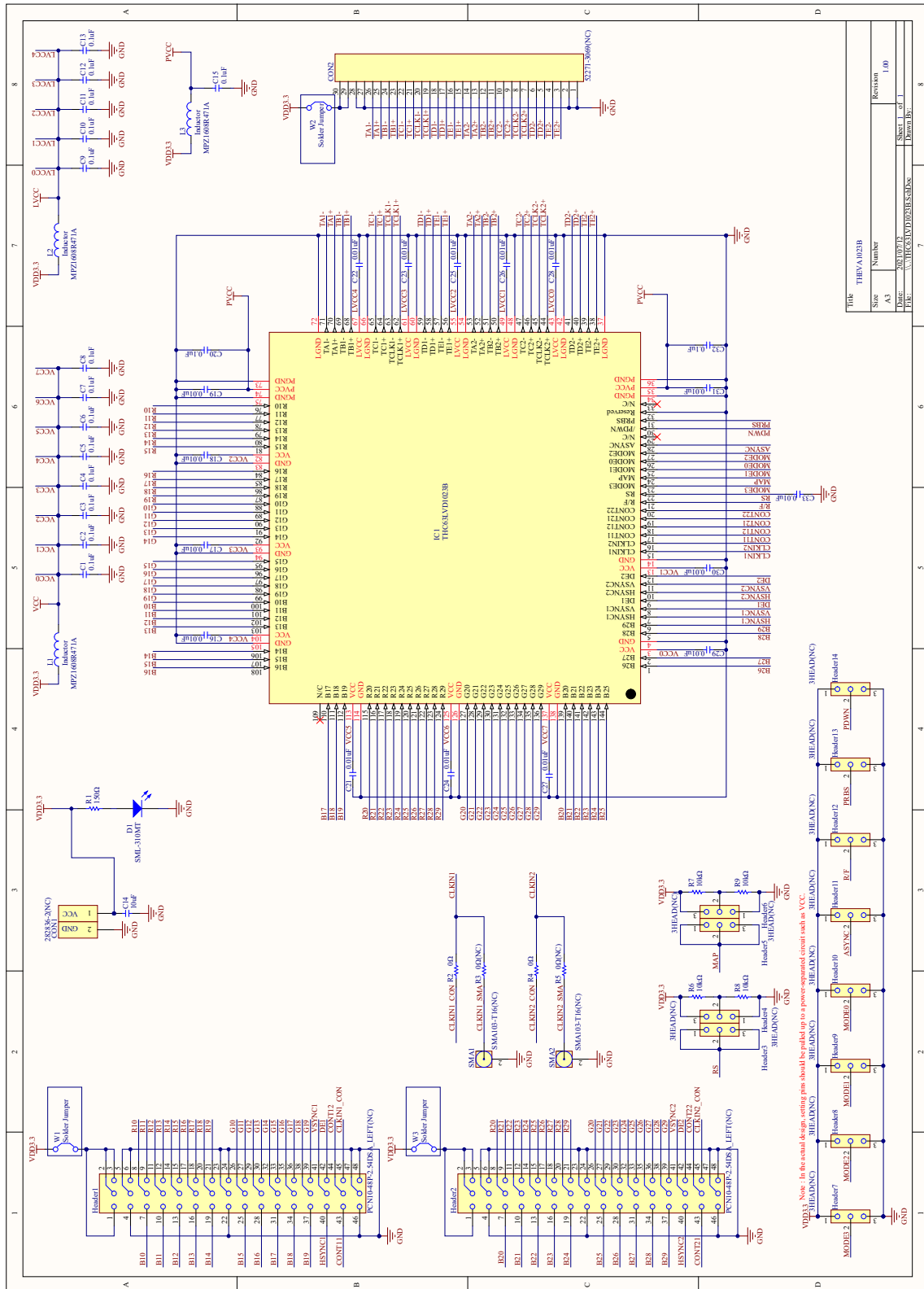
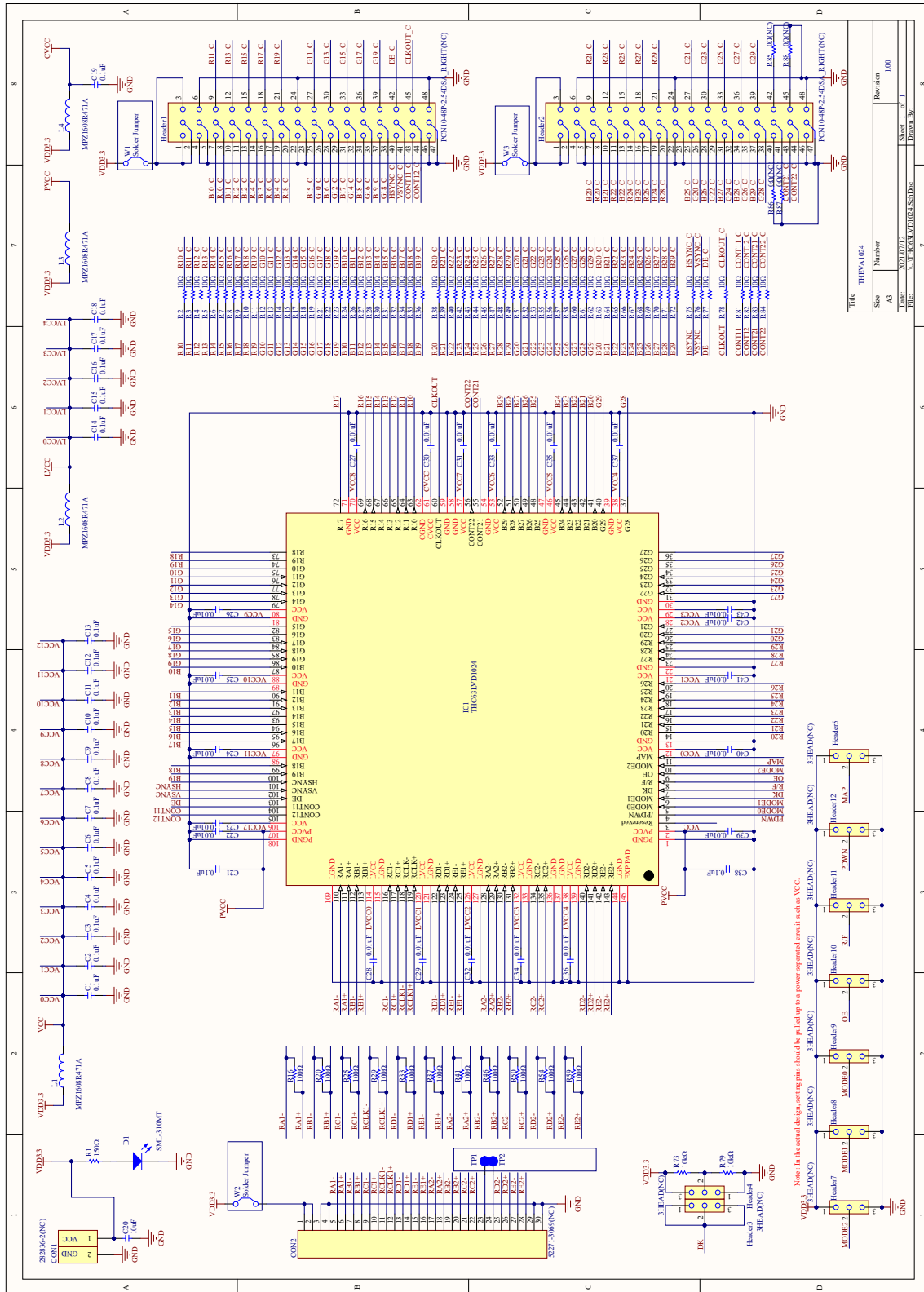


Figure 10 THEVA1023B Schematic



File	Size	Number	Revision
THEVA1024.DWG	83	2021/07/17	100
FILE: \\TCES\AV\1024.SDS			Sheet 1 of 1
			Drawn By:

Figure 11 THEVA1024 Schematic

8. Bills of Materials

Table 3 THEVA1023B BOM

TYPE	Value / Part No.	Package	SPEC	Reference No.	Qty	Note
Capacitor	0.1uF	1005	16V	C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C15, C20, C32	17	
Capacitor	10uF	2012	16V	C14	1	
Capacitor	0.01uF	1005	16V	C16, C17, C18, C19, C21, C22, C23, C24, C25, C26, C27, C28, C29, C30, C31, C33	16	
Connector	282836-2(NC)	5mm_pitch	2pin	CON1	1	
Connector	52271-3069(NC)	1mm_pitch	30pin	CON2	1	
Connector	PCN10-48P-2.54DSA_LEFT(NC)	2.54mm_pitch	48pin	Header1, Header2	2	
Connector	SMA103-T16(NC)	1.6mm	PCB End Jack	SMA1, SMA2	2	
Header	3HEAD(NC)	2.54mm_pitch	---	Header3, Header4, Header5, Header6, Header7, Header8, Header9, Header10, Header11, Header12, Header13, Header14	12	
IC	THC63LVD1023B	LQFP144	---	IC1	1	
Inductor	MPZ1608R471A	1608	1.2A	L1, L2, L3	3	
LED0	SML-310MT	1608	GREEN	D1	1	
Resistor	150Ω	1005	0.1W	R1	1	
Resistor	0Ω	1005	0.1W	R2, R4	2	
Resistor	0Ω(NC)	1005	0.1W	R3, R5	2	
Resistor	10kΩ	1005	0.1W	R6, R7, R8, R9	4	

Table 4 THEVA1024 BOM

TYPE	Value / Part No.	Package	SPEC	Reference No.	Qty	Note
Capacitor	0.1uF	1005	16V	C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14	21	
Capacitor	10uF	2012	16V	C20	1	
Capacitor	0.01uF	1005	16V	C22, C23, C24, C25, C26, C27, C28, C29, C30, C31, C32, C33, C34, C35, C36, C37, C39, C40, C41, C42, C43	21	
Connector	282836-2(NC)	5mm_pitch	2pin	CON1	1	
Connector	52271-3069(NC)	1mm_pitch	30pin	CON2	1	
Connector	PCN10-48P-2.54DSA_RIGHT(NC)	2.54mm_pitch	48pin	Header1, Header2	2	
Header	3HEAD(NC)	2.54mm_pitch	---	Header3, Header4, Header5, Header6, Header7, Header8,	10	
IC	THC63LVD1024	LQFP144	---	IC1	1	
Inductor	MPZ1608R471A	1608	1.2A	L1, L2, L3, L4	4	
LED0	SML-310MT	1608	GREEN	D1	1	
Resistor	150Ω	1005	0.1W	R1	1	
Resistor	10Ω	1005	0.1W	R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R17, R18, R19, R21, R22, R23, R24, R26, R27, R28, R30, R31, R32, R34, R35, R36, R38, R39, R40, R42, R43, R44, R45, R47, R48, R49, R51, R52, R53, R55, R56, R57, R58, R60, R61, R62,	68	
Resistor	100Ω	1005	0.1W	R16, R20, R25, R29, R33, R37, R41, R46, R50, R54, R59	11	
Resistor	10kΩ	1005	0.1W	R73, R74, R79, R80	4	
Resistor	0Ω(NC)	1005	1A	R85, R86, R87, R88	4	

9. Set Items

Table 5 Set Items

TYPE	Part No.
DC Connector	282836-2
FFC Connector for LVDS Link	52271-3069
FFC 30pin 1mm Pitch for LVDS Link	98267-0475
Pin Header	---

It's possible to mount these parts on this board and use.

10. Notices and Requests

Please kindly read, understand and accept this “Notices and Requests” before using this product.

For the Material:

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2. The circuit diagrams described in this material are examples of the application which may not always apply to design of respective customers. THine Electronics, Inc. (“THine”) is not responsible for possible errors and omissions in this material. Please note even if the errors or omissions should be found in this material, THine may not be able to correct them immediately.
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3. This product is not radiation-tolerant product.
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7. Customers are asked, if required, to judge by themselves on whether this product falls under the category of strategic goods under the Foreign Exchange and Foreign Trade Act.
8. Please Note that even if infringement of any third party’s industrial ownership should occur by using this product, THine will be exempted from any responsibility unless it directly relates to the production process or functions of the product.
9. Developing, designing and manufacturing of customers’ own products, equipment or system by using of this product is strictly prohibited in any way.

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